BNC

Digital Delay Generators
Models 7065 and 7075

INSTRUCTION MANUAL

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BERKELEY NUCLEONICS CORPORATION
1198 Tenth St., Berkeley, California 94710

Warranty

Berkeley Nucleonics Corporation warrants all instruments, including component parts, to be free from defects in material and workmanship, under normal use and service for a period of one year. If repairs are required during the warranty period, contact the factory for component replacement or shipping instructions. Include serial number of the instrument. This warranty is void if the unit is repaired or altered by others than those authorized by the Berkeley Nucleonics Corporation.

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Digital Delay Generator
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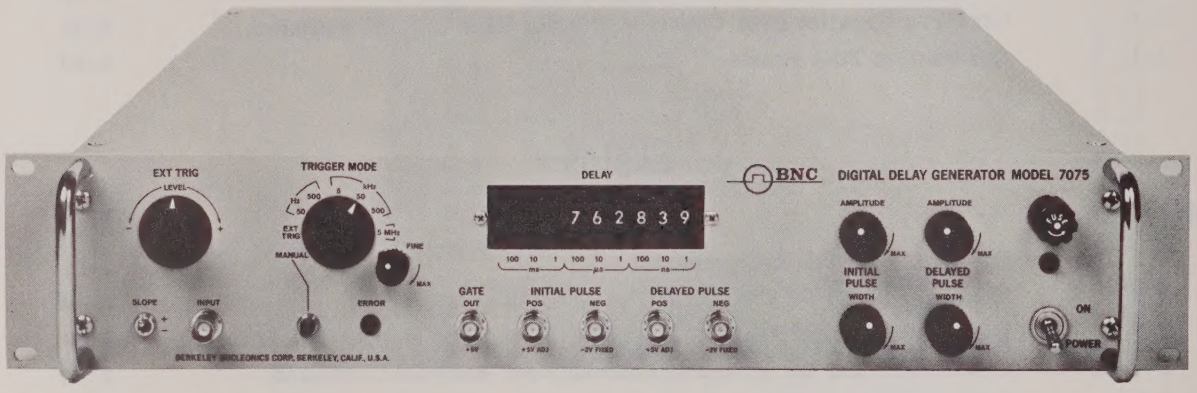

The Models 7065 and 7075 are precision instruments that provide time delays from 0 to 999.999 μs or, with Option A, to 999.999999 ms. Delays are selectable in 1 ns increments. A gate output equal to the delay time is also provided.

The Model 7065's Initial and Delayed Pulse outputs are fixed in amplitude and width, while the Model 7075 includes continuously variable width and amplitude controls as well as self-triggering up to 5 MHz. External triggering is accomplished with the ±2 volt threshold range selector for both positive or negative-going slopes. A ± one-half clock period indeterminacy between the trigger and output pulses is automatically eliminated by trigger synchronizing circuitry that reduces indeterminacy to zero.

Both instruments have an error warning light to signal excessive (error producing) triggering rates relative to the time settings. Remote programming and external time base connection are optionally available.

SECTION 1

SPECIFICATIONS

DELAY AND GATE SELECTION	(Gate min. 10 ns) 0 to 999.999 μs in 1 ns increments. See Option A for extension up to 1 second.
ACCURACY	
Delay:	1 - 9 ns, ±0.1 ns; 10 - 99 ns, ±0.3 ns; 100 ns to full range, ±0.5 ns ± time setting x time base error.
Gate:	Delay interval ±2 ns (fixed).
TIME BASE STABILITY	
Aging:	±100 ps ±2 x 10^{-7} per week.
Temperature:	<1 x 10^{-6}, 0 - 50° C.
INSERTION DELAY	Between Trigger and Initial Pulse: 85 ns.
INDETERMINACY	None.
JITTER	
Between External Trigger and Initial Pulse:	30 ps rms max.
Between Initial and Delayed Pulses:	1 to 999 ns, 100 ps rms max; 1 to 999 μs, 150 ps rms max; 1 ms to 999 ms (Option A), 250 ps rms max ±1 x 10^{-8} x delay.
TRIGGER MODES	
External:	Rate 0 to 5 MHz; 10 ns minimum width; 200 mV minimum amplitude; 50 Ω nominal input impedance. Trigger level control ±2 V, continuously adjustable. Positive or negative slope selection switch.
Manual:	Panel pushbutton.
Internal (Model 7075 only):	5 Hz to 5 MHz continuously adjustable through five ranges.
OUTPUT PULSES	
Initial and Delayed: (Model 7065)	Positive, +5 V into 50 Ω; Negative, -2 V from 50 Ω; 3 ns rise and fall times; 40 ns width, may be altered.
Initial and Delayed: (Model 7075)	Positive, +0.1 to +5 V into 50 Ω, continuously adjustable; Negative, -2 V from 50 Ω; 3 ns rise and fall times; 15 ns to 1 μs width, continuously adjustable.
Gate:	+5 V into 50 Ω; 3 ns rise and fall times.
CLOCK MODES	
Internal:	Operates from internal oscillator.
External:	See Option B for operation from an external frequency standard.

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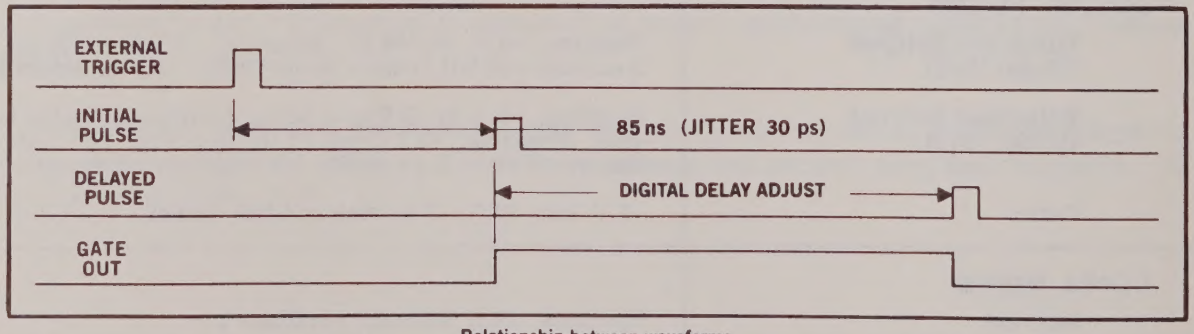
DIMENSIONS Rack Mount:	19" W x 3-1/2" H x 19-3/4" D (483 x 89 x 502 mm).
WEIGHT Model 7065: Model 7075:	18 lbs net (8.2 kg); 24 lbs (11 kg) shipping. 19 lbs net (8.6 kg); 24 lbs (11 kg) shipping.
AMBIENT	0^{o} C to 50^{o} C (32^{o} F to 122^{o} F).
POWER Model 7065: Model 7075:	115/230 V ± 10%, 50/60 Hz, 85 W. 115/230 V ± 10%, 50/60 Hz, 90 W.
OPTIONS A: Extended Range	Three additional decades extend Delay and Gate range to 999.999999 ms.
B: External Clock	Instrument may be phase locked to an external frequency standard. TTL input of 40 ns minimum width, either 1 MHz or 10 MHz.
P1: BCD Remote Programming	Time settings are remotely selectable. Coding is TTL/DTL compatible, V(High) = 0, V(Low) = 1. Buffer storage provided. Data Strobe, V(Low) = Strobe. Remote/Local, V(High) = Local; V(Low) = Remote. Programming Time: 1 μs max. Chassis connector: Amphenol 57-40500.
P2: GPIB Remote Programming	For automatic selection of time settings. Complies with IEEE Std. 488-1978. Non-pollable. Includes internal RAM for bus-storing locally up to sixteen 6 or 9-digit (Option A) settings.



Relationship between waveforms

FIG. 1-1. Time Delay Setting.

SECTION 2

OPERATING INFORMATION

2.1 GENERAL

This section will familiarize the user with the preparation, capabilities and operation of BNC Models 7065 and 7075 Digital Delay Generators. Operating controls and connectors, as well as operating procedures will be covered. The term General Purpose Interface Bus (GPIB) is used to describe the IEEE 488-1978 Standard. In this context, hexadecimal numbers will be enclosed by " " and decimals numbers by ' '.

2.1.1 MODEL DIFFERENCES

This instruction manual applies to both the Model 7065 and Model 7075. The instruments are similar in construction, performance, etc. The exceptions being the Model 7075 is somewhat more flexible application-wise due to its self-triggering capability and output pulse adjustments. Information in this manual distinguishes between the two models when their differences are of likely significance to the user.

2.1.2 PERFORMANCE INFORMATION

(1) The circuitry of Models 7065 and 7075 synchronizes the internal clock with external or internal triggers to provide outputs devoid of the clock uncertainty normally found in counting circuits. In this manner, outputs are generated with no indeterminacy with respect to the input trigger. With the addition of Option B (Para. 2.2.17), the internal clock reference of these units may be locked to an external standard of either 1 MHz or 10 MHz to obtain extremely stable and accurate delays and widths.

(2) Time measurements between signal edges of outputs and inputs for the units are specified for the 50% amplitude points of the pulses. Rise and fall time measurements are specified for the 10% and 90% points of each waveshape. All timing signal figures are expressed as produced at the appropriate connector on the front panel. Care must be taken to match external cables for propagation times if the accuracy of the unit is to be maintained.

2.1.3 OPERATING TEMPERATURE

(1) The internal frequency source of the instrument is enclosed in a fast warm-up oven. An instrument should be allowed to warm up for 10 to 15 minutes before high precision measurements are made. Less critical tests can be performed immediately after turn-on.

(2) The unit has a fan for cooling. In the unlikely event that the fan stops and the internal ambient temperature is too high, the instrument will automatically shut down. Thus, if the unit stops

for no apparent reason, and the display is dark, check for excessively high temperature and/or a blockage of the fan before taking other steps. The fuse should also be checked. If high ambient and/or a fan problem is discovered, reducing the temperature and/or unblocking the fan will automatically allow resumption of operation.

2.1.4 CABLES, ATTENUATORS AND OSCILLOSCOPES

The outputs of the Models 7065 and 7075 contain frequency components in excess of 100 MHz. All signal handling components such as loads, attenuators, cables, connectors and oscilloscopes should be able to pass these signals without distortion in order to maintain and observe the inherent accuracy of the unit.

NOTE

Some sampling oscilloscopes have maximum input ratings that may be exceeded by the outputs of the instrument. When using such equipment be sure to turn down the Amplitude control or use an attenuator to lower the signal to a level safe for the oscilloscope.

As the reference points for calibration are directly at the input and output connectors and at the 50% points of the waveshapes, the effect of cables in both distorting and delaying the signals is important. Such phenomena should always be considered when making critical timing measurements. For example, one foot of RG58/U cable has a delay of 1.5 ns. Therefore, if cables from the outputs are different in length by only 1.5 inches, the error induced will be greater than ±100 ps, the inherent accuracy of the instrument. Also, should a mismatch occur with one of the cables, it is possible that reflections could occur at the 50% points of the pulses thereby adding another source of error.

2.2 OPERATING CONTROLS AND CONNECTORS

2.2.1 LINE VOLTAGE AND 115/230 SWITCH (Rear Panel)

The instrument can operate from either a 115-volt or a 230-volt, ±10%, 50/60 Hz line source. A slide switch on the rear panel selects either of the line voltages. The switch is preset at the factory for the line voltage of the country to which the instrument is shipped. This switch should not be moved unless the line voltage is changed. When the switch is moved, the fuse should be changed to the proper value for the new line voltage (Para. 2.2.2).

WARNING

IN THE EVENT THAT A TWO-WIRE ADAPTER OR OTHER CONNECTOR IS USED, CONNECT THE CHASSIS OR GREEN WIRE TO A SUITABLE EARTH GROUND TO ELIMINATE SHOCK HAZZARD.

2.2.2 POWER SWITCH AND FUSE

All primary power is applied through the POWER ON toggle switch on the front panel. The pilot lamp should light when the unit is turned on. If the switch is in the ON position and the lamp is not lighted, it may be that either the fuse is blown or the unit is in an excess temperature condition owing to a fan problem or an excessively high internal temperature. Should the latter be the case, cooling the unit and/or restoring fan performance will restore normal operation as soon as the internal temperature of the unit reaches a safe level. For 115 VAC operation the correct fuse value is 1.5 amp, Slo-Blo while for 230 VAC operation it is 0.75 amp, Slo-Blo.

2.2.3 EXTERNAL TRIGGER INPUT

When the TRIGGER MODE switch (Para. 2.2.6) of the Model 7075 is in the EXTernal TRIGger position, a signal of the proper levels to this connector will trigger the instrument. The Model 7065 is without a Trigger Mode selection switch and therefore is always set up for external triggering. The input impedance for both models is 50 ohms. For proper triggering the input signal must be at least 200 mV peak-to-peak amplitude, at least 10 ns wide and 5 MHz or less in frequency. Peak inputs should not exceed + or - 15 volts and the average power of the input should not exceed 0.5 Watt.

2.2.4 EXTERNAL TRIGGER SLOPE SWITCH

The SLOPE switch determines whether the instrument will trigger on a positive-going or negative-going transition at the EXTernal TRIGger INPUT (Para. 2.2.3) connector. Use this switch in conjunction with the trigger level control described below.

2.2.5 EXTERNAL TRIGGER LEVEL CONTROL

The EXTernal TRIGger LEVEL control determines the voltage level at which the instrument will trigger. The Level control varies the threshold from $> +2$ volts when fully clockwise to < -2 volts fully counterclockwise. For a positive transition, triggering occurs when the input signal passes through threshold by at least 100 mV, and retriggering can be effected after the input signal has dropped at least 100 mV below threshold. For a negative transition, the operation is the same but the directions are reversed. This control can be an aid to precisely match the timing of two or more instruments (Para. 2.3.5).

2.2.6 TRIGGER MODE SWITCH AND FINE CONTROL (Model 7075 only)

The TRIGGER MODE switch selects the operating mode: Manual Trigger, External Trigger or Internal Trigger. In the MANUAL position, each time the MANUAL button is pressed a single delay and gate cycle is produced. In the EXTernal TRIGger position, the EXTernal TRIGger INPUT connector (Para. 2.2.3) is enabled and signals of the proper levels will trigger the Model 7075.

In the remaining positions, an internal repetition rate generator is used to trigger the unit. Six switch positions select overlapping decade frequency ranges from 50 Hz to 5 MHz. The FINE control adjusts the frequency over a 10:1 swing within each range to provide continuous coverage from 5 Hz to 5 MHz.

2.2.7 MANUAL TRIGGER PUSHBUTTON

The MANUAL trigger pushbutton generates one delay and gate cycle each time it is pressed. If the button is pressed during a timing cycle in progress, there is a chance that an erroneous output will occur. To use this control on the Model 7075, the TRIGGER MODE switch must be in the MANUAL position.

2.2.8 ERROR LIGHT

Whenever the period of the trigger signal (either from the internal repetition rate generator or from external triggering) is shorter than the delay time setting, the error LED will light and stay on as long as the excessively fast triggering rate persists. If a trigger timing error occurs only once or occasionally, the light will blink on approximately 100 ms for each fault. If Option B is present, see Para. 2.2.18.

2.2.9 DELAY SWITCHES

The DELAY switches set the delay between the Initial and Delayed pulses and the Gate time. A timing range from 0 to 0.999999 ms is standard. Option A provides a range to 999.999999 ms. If a DELAY switch is reset during a delay cycle, the next trigger (external or internal) will generate the new time delay and gate. However, should a change be made in the interval between delays, the next trigger after the change will cause one delay and gate output with the previous time setting. Subsequent outputs will be of the new setting.

If a remote programming option is installed, and in use, the new delay or gate can be implemented immediately by bringing the Reset line low (Para. 2.3.6 or 2.3.7).

2.2.10 INITIAL POSITIVE OUTPUT

An Initial Pulse occurs at the beginning of each delay cycle and is issued from the INITIAL PULSE POSitive connector. When zero delay is set with the DELAY switches, the leading edge of the Delayed pulse rises at the same time as the start of the Initial pulse. The Initial pulse is +5 volts maximum in amplitude into a 50-ohm load from a low impedance source. Both its amplitude and width are variable in the Model 7075. See Para. 2.2.14 and Para. 2.2.15.

In the Model 7065 this output is fixed in amplitude at +5 V and 40 ns width. See Para. 2.2.12 for information on changing the pulse width.

Note that the best pulse shapes are obtained when this output is terminated into 50 ohms. If a higher impedance is to be used, better results are obtained if a parallel resistance is used at the load to simulate 50 ohms. Similarly, a series resistance should be used if the load is less than 50 ohms.

2.2.11 INITIAL NEGATIVE OUTPUT

This negative pulse is coincident with the positive Initial Pulse. Its amplitude is fixed at -2 volts from a 50-ohm source so that when a 50-ohm load is used, the amplitude is -1 volt. The output can be converted to ECL levels by terminating in 50 ohms and using an external resistor that sources 30 mA to a negative supply.

The width of this pulse from the Model 7075 is variable together with the positive Initial Pulse output. In the Model 7065 the width is normally fixed at 40 ns but can be changed per Para. 2.2.12.

2.2.12 DELAYED POSITIVE OUTPUT

A Delayed Pulse marks the end of the time delay determined by the Delay setting or remote programming and is available from the DELAYED PULSE POSitive connector. The characteristics of this output pulse for the two models are the same as those of the Initial Pulse (see Para. 2.2.10).

For some users of the Model 7065, the normal 40 ns width of both the Initial and Delayed pulses may be inappropriate. If so, the user can change either or both by referring to Schematic 7065-32 and the following procedure: remove either or both R58, R99 and add either or both Q2, Q3 and associated components shown within the dashed line box(es). The circuit board has provision for adding the parts. A fixed resistor of correct value to give the appropriate pulse width can be substituted for variable R804/R806.

2.2.13 DELAYED NEGATIVE OUTPUT

This negative pulse is coincident with the Positive Delayed Pulse. The characteristics of this output pulse for the two models are the same as those of the Negative Initial Pulse (see Para. 2.2.11).

2.2.14 AMPLITUDE CONTROLS

The AMPLITUDE controls are two adjacent knobs that independently set the Initial and Delayed pulse output levels. They vary their respective outputs from < +0.5 volt to > +5.0 volts when the outputs are terminated into 50 ohms. The respective NEGative outputs are not affected by these controls.

2.2.15 WIDTH CONTROLS

The WIDTH controls are two adjacent knobs that independently vary the widths of the Initial and Delayed outputs. The INITIAL PULSE control varies both its positive and negative outputs simulta-

neously through a 15 ns to 1 μs range. The DELAYED PULSE control varies both of its outputs through a similar range of widths.

2.2.16 GATE OUTPUT

The GATE OUTput is a fixed +5 volt pulse that rises with the leading edge of the Initial Pulse and falls with the leading edge of the Delayed Pulse and therefore equals the duration of the delay setting. The Gate output is coincident with the above pulses to within a fixed accuracy of ±2 ns. "Fixed" here means any error in coincidence is constant throughout all delay settings for a specific instrument.

2.2.17 EXTERNAL CLOCK SWITCH (Option B—Rear Panel)

When Option B is installed in the Model 7065 or 7075, this switch determines whether a 1 MHz or 10 MHz signal to the EXTernal CLOCK input will be used as the reference frequency. If the switch is in the wrong position, i.e., the input to the EXTernal CLOCK connector does not correspond to the switch setting, the front panel Error LED will come on (Para. 2.2.18).

2.2.18 EXTERNAL CLOCK INPUT (Option B — Rear Panel)

Option B provides the user with the capability of phase locking the internal frequency reference system of the Model 7065 or 7075 to an external frequency standard that is within $\pm 1 \times 10^{-5}$ of 1 MHz or 10 MHz. This allows the generation of long time delays and gates with accuracies mainly limited by the precision of the external frequency standard used.

The EXTernal CLOCK connector on the rear panel is the input for the external frequency standard. The frequency to be used is selected by the 1 MHz/10 MHz toggle switch. The signal must have TTL compatible levels and a minimum pulse width of 40 ns. This input has a high impedance; therefore, low impedance signals should be properly terminated.

If there is no signal at rear panel EXTernal CLOCK input, the instrument's internal 100 MHz clock count will be locked to the unit's own internal crystal reference. The accuracy of outputs will then depend on the stability of this time base. When a suitable TTL-level signal of 1 MHz or 10 MHz is available at External Clock input, the unit will automatically detect this signal and lock its clock circuit to it, provided the applied reference is within ±1 part in 10^5 of the nominal 1 MHz or 10 MHz frequency. The accuracy of the delays and gates produced by the instrument will now reflect the accuracy of the external time base. That is, if the switch is set to 1 MHz, the unit will lock to a signal of 1 MHz ±10 Hz. If the switch is set to 10 MHz, the unit will lock to a signal of 10 MHz ±100 Hz. (Note: regardless of which frequency is selected, the internal clock, when locked to the external signal, will have a frequency of 100 MHz ± the accuracy of the applied signal.) Should the external reference deviate from the selected nominal frequency by more than 1 part in 10^5 in either direction, the error LED will light indicating the instrument is no longer locked to the external time base.

During this condition, the internal clock of the instrument will cause an error of about 1 part in 10^5 in the direction of the applied signal's deviation. For example, with the external clock switch set to 1 MHz, if the applied reference signal is 1.000020 MHz, the unit's internal clock will be running approximately 1 part in 10^5 fast, resulting in outputs that are short by 1 part in 10^5.

If the error LED lights when an external frequency reference is applied, first check that the 1 MHz/ 10 MHz switch is in the appropriate position. If the LED remains on, remove the external signal from the External Clock connector. If the LED goes off, it probably indicates that the external signal is not within the required 1 part in 10^5 range. If the LED remains lit after the reference signal has been removed, it probably indicates that the error condition is a trigger timing error. If the applied frequency is grossly below 1 MHz (e.g., < 900 kHz) or above 10 MHz, the instrument won't detect it and an Error indication will not appear.

An error signal produced when the External Clock input signal frequency is incorrect will appear on the GPIB SRQ line if the Error Out rocker (rear panel) is in the ON position and the unit is in the Remote mode. Since the instrument cannot respond to a poll, this function should be used with caution. See Para. 2.3.7.5.

2.2.19 PROGRAM IN CONNECTOR (Option P1— Rear Panel)

When equipped with BCD programming Option P1, the instrument is fitted with a 50-pin connector that serves for all data and control signals used to remotely program and control the instrument. The mate for the connector on the rear panel is Amphenol P/N 57-30500. See Para. 2.3.6 for P1 operating details.

2.2.20 PROGRAM IN CONNECTOR (Option P2 — Rear Panel)

An instrument with programming Option P2 is fitted with a 24-pin connector that conforms to the IEEE-488 1978 General Purpose Interface Bus (GPIB) Standard using metric hardware. This connector serves for all data and control signals used to remotely program and control the instrument. Identification of the applicable hardware, etc., is covered in the text of the IEEE-488 Standard and other readily available literature on this popular programming scheme. Refer to Table 2-2 for pin assignments and Para. 2.3.7 for P2 operating details.

2.2.21 ADDRESS/ERROR SWITCHES (Option P2 — Rear Panel)

The five rockers on the left of this eight-section DIP switch, marked 5...1, are used to set the instrument address for GPIB use. Any address from "0" to "30" is allowable.

The ERROR OUT switch determines whether or not the unit puts an output on the GPIB SRQ line when the front panel ERROR light is on. See Para. 2.2.18 and 2.3.7.5 for details.

NOTE: This output capability does not strictly adhere to the IEEE 488-1978 Standard because the instrument is not capable of responding to a poll.

It is advisable to use this output signal with caution. It is provided to assist the user in debugging a system or whenever the inability to determine which device is causing an interrupt is not a problem.

The two rockers marked "A" and "B" are for setting up remote reset timing for Option P2. See Para. 2.3.7.5A for details.

2.2.22 LOCAL/REMOTE SWITCH (Option P2 — Rear Panel)

This switch determines whether the instrument is under front-panel switches(Local) or GPIB programming (Remote) operating control. When in the Local position, the unit's time settings are selectable only with the Delay switches. In Remote, the unit is enabled to operate from the GPIB.

NOTE

The instrument will remain in the Local operating mode until it is addressed by a controller of the GPIB. The unit then remains in the Remote mode until the switch is returned to Local or its power is turned off. The instrument cannot be returned to the Local mode by the GPIB.

2.3 OPERATING INSTRUCTIONS

2.3.1 GENERAL

Familiarize yourself with the controls and connectors described in the first part of this section before attempting to operate the instrument for the first time. Also, it is important to be aware of the information on performance and operating conditions in Para. 2.1.2, 3 and 4 to get the most out of the Models 7065 and 7075. The following material tells how to operate the unit locally by hand or by remote programming if equipped with Option P1 or P2.

2.3.2 TURN-ON

Measurements with accuracies better than 10 ppm require that the instrument be allowed to warm up for at least 15 minutes. If accuracies on the order of 0.01% are satisfactory, the unit can be used immediately after turn-on.

2.3.3 INSERTION DELAY

There is a fixed throughput time from the instant of triggering to the leading edge of the Initial Pulse. This is called the Insertion Delay and is nominally specified as 85 ns. This fixed figure may vary somewhat from one instrument to another. Therefore, if the timing application is critical and referenced to the input trigger (rather than the Initial Pulse) you may wish to determine the exact duration of the insertion delay for the specific instrument in use. The added insertion delay is a consideration for any delay or gate that starts being timed from a trigger pulse.

2.3.4 TIME DELAY AND GATE GENERATION

If an instrument is to be checked to verify it is basically functioning, a trigger source and an oscilloscope or time interval meter (TIM) can be used. Connect an external trigger source of between 200 mV and 5 V amplitude to the EXT TRIG INPUT connector, appropriately set the SLOPE and LEVEL controls and a short delay setting after which the unit should begin to operate by producing output pulses as observed with the scope or TIM.

If an indicating instrument is not available to check the actual outputs, and provided the trigger rate is greater than 1 kHz, the ERROR light may be used to indicate the Delay Generator is at least responding to external triggering by the following procedure:

1. Adjust the DELAY thumbwheel switches to a setting of 999999 ns and provide the > 1 kHz triggering.

2. Turn the LEVEL control fully back and forth if necessary to start triggering. The ERROR lamp should light, which indicates the instrument is triggerable.

3. Set in a short delay and the ERROR lamp should go out since the trigger period is now greater than the Delay setting (Para. 2.2.8).

With Option A supplied, the same procedure can be used for trigger rates as low as 1 Hz. Simply set the thumbwheel switches to 999999999 ns and proceed in a similar fashion as above starting with a trigger rate of > 1 Hz.

When operating the instrument for an actual application, keep in mind that the time delay setting controls the interval between the leading edges of the Initial Pulse (T_0) and Delayed Pulses (T_1). See Fig. 1-1. Time control that starts a period from the input trigger pulse must take into account the instrument's fixed insertion delay. The Gate output is timed to coincide with the Initial and Delayed pulses' leading edges so its "on" interval equals, within prescribed specifications, the Time Delay setting.

2.3.5 MULTIPLE DELAYS AND GATES

Because the Model 7065 and 7075 exhibit very low jitter when triggered, multiple units may be used to generate parallel or sequential delays and gate widths with very low jitter between pulse edges.

With parallel operation, all units are triggered from the same source. If identical cables are used, the outputs from all units will be very close in coincidence for the same time settings. Depending upon the rise time of the triggering source, the outputs can be even more closely matched by adjustment of the individual Trigger Level controls. This will cause the various units to trigger at different points on the input waveform which slightly changes the insertion delay(s) to attain matched timing.

For serial or sequential operation, the first unit can be triggered from an external source (or, if desired, internally with Model 7075). The next instrument is then triggered from the delayed output of the first and so on. This procedure may be used for any number of units desired. If the Gate Output of the second unit is used, the output pulse obtained is precisely settable in both delay and width, with very low jitter between output pulse edges and from those edges to the trigger. Note that the insertion delay of each instrument will be a consideration (an addition) to its time setting.

2.3.6 REMOTE PROGRAMMING — OPTION P1

When Option P1 is installed, a 50-pin connector is added to the rear panel. The connector is the input point for all data and control signals used to remotely program and control the instrument. Each input lead exhibits the behavior of one standard TTL gate with a 22-kilohm pull-up resistor connected to +5 volts.

1. Delay Data Inputs

   The delay data inputs determine the delay interval when the unit is in the remote mode. Data is entered in parallel BCD format with V(high) = logical 0 and V(low) = logical 1. Table 2-1 provides the programming pin number assignments.

2. Strobe Pulse

   A strobe pulse is used to transfer the data from the data lines to the internal memories of the two models. When the strobe line is at V(high), the unit will ignore signals on the data lines. Conversely, when the strobe is low, the internal memory follows the data lines. But, when the strobe line returns high, the data present at the time is retained in the memory.

   Neither the Model 7065 or 7075 will recognize the new data in the latches until the end of a delay cycle. In the event the unit is strobed during a delay cycle, the next delay will reflect the new data. Accordingly, if the unit is strobed between a delay cycle, the next delay will be determined by the old data, while the second delay after the strobe will be determined by the new data. If the data must be transferred between cycles, and immediate update is necessary, the transfer can be made by bringing the reset line low after the strobe has occurred (Para. 3, below).

   NOTE

   If an occasional inappropriate delay is not acceptable, the unit should not be strobed within ±100 ns of the leading edge of the delayed pulse since false data loading may occur. (Minimum strobe width is 100 ns.) Data must be present and correct for 25 ns before and after the end of the strobe pulse. The strobe-signal (data strobe) pin assignment is shown in Table 2-1.

Table 2-1. P-1 Connector Pin Assignments.

DELAY INCR.	PIN NO.
1 ns	1
2 ns	2
4 ns	26
8 ns	27
10 ns	3
20 ns	4
40 ns	28
80 ns	29
100 ns	5
200 ns	6
400 ns	30
800 ns	31
1 μs	7
2 μs	8
4 μs	32
8 μs	33

DELAY INCR.	PIN NO.
10 μs	9
20 μs	10
40 μs	34
80 μs	35
100 μs	11
200 μs	12
400 μs	36
800 μs	37
*1 ms	13
*2 ms	14
*4 ms	38
*8 ms	39
*10 ms	15
*20 ms	16
*40 ms	40
*80 ms	41

DELAY INCR.	PIN NO.
*100 ms	17
*200 ms	18
*400 ms	42
*800 ms	43
ERROR OUTPUT	23
RESET	24
DATA STROBE	25
LOCAL/REMOTE	49
GROUND	50

*These delay increments available with Option A only.

Remote programming connector (J901) is an Amphenol 57-40500 and requires a mating connector Amphenol 57-30500

3. Reset

The reset signal stops any delay cycle in progress and activates data transfer, for immediate use, from the memory to the internal counters. If the unit receives both a strobe and a reset signal, the next delay cycle will reflect the latest data.

V(low) is the level for reset. Table 2-1 illustrates the pin assignments. Minimum reset width is 100 ns.

4. Local/Remote Control

A low level on this line causes the Models 7065 and 7075 to operate in the Remote mode with control furnished from a remote source. When the Local/Remote line is high or left open, operation is in the Local mode from the front-panel DELAY switches. The memory is disabled, and the Strobe and Reset lines have no effect.

V(low) = remote and V(high) = local. Table 2-1 shows the pin assignment.

5. Error Output

Whenever the front-panel Error light is on, it indicates that the error output

line is low. See Para. 2.2.8 for additional details. If the error condition is continuous, the output will be DC level. If the error occurs intermittently, the output will be a negative-going pulse of approximately 100 ms duration. Table 2-1 shows the pin assignment.

2.3.7 REMOTE PROGRAMMING — OPTION P2

2.3.7.1 INTRODUCTION

Option P2 modifies the Models 7065 and 7075 such that their operation conforms to the IEEE Standard 488-1978 — General Purpose Interface Bus (GPIB) — as applies to "listener-only" instruments.

A complete description of the IEEE standard is beyond the scope of this manual. For any additional information, refer to the Standard itself or the many other publications which cover the GPIB. In the following text, hexadecimal symbols will be enclosed by " " and decimals by ' '.

2.3.7.2 THE IEEE STANDARD 488-1978 (GPIB)

This standard is a byte-serial, bit-parallel interface system designed for use with various combinations or systems of programmable instruments. As a standard, the 488-1978 defines specifications for all circuits, cables, connectors, and control protocol to allow unambiguous transfer data between devices. (See Table 2-2.)

It is worth noting, however, that the GPIB has several operating constraints and limits—specifically:

A. No more than fifteen (15) devices can be interconnected by a single contiguous line.

B. Total data line transmission length is limited to 20 meters, or two meters times the number of devices occupying the bus, whichever is the less.

C. The data rate through any signal line must be less than, or equal to, one Megabit per second.

D. All data exchange is digital.

The system transfers data between components along 16 transmission lines—eight data bus lines for transmitting characters in a byte-serial, bit-parallel fashion, three byte transfer control or handshake lines, and five general interface management signal lines.

Figure 2-1 offers a more detailed description of the GPIB design and operation. The following description of the sixteen bus lines is included here, however, to provide a convenient reference for the Model 7065 and 7075 user.

Data Bus (Message) Lines

DIO-1 - DIO-7 DATA INPUT/OUTPUT

These are the seven data bus lines or message lines. Depending on the condition of the ATN (Attention) line, these lines carry either data or address information.

Handshake Lines

DAV (Data Valid)

This line indicates that data is present on the DIO lines, and is one of three handshake lines used to indicate the availability and validity of DIO information.

NRFD (Not Ready for Data)

This is a handshake line which indicates whether all devices are, or are not, ready to accept data.

NDAC (Not Data Accepted)

This third handshake line is used to indicate that data has been accepted by all devices.

Bus-Management Lines

ATN (Attention)

The ATN line is one of the bus management lines. It is used to specify the manner in which data line information is interpreted, and it also specifies the devices that must respond. When ATN is true, the DIO lines carry addresses or commands. When false, the lines carry data.

IFC (Interface Clear)

This bus management line places the system in a quiescent state (i.e., talk and listen devices are idled).

SRQ (Service Request)

SRQ is also a bus management line and is used by a device to indicate the need for service and request an interrupt.

REN (Remote Enable)

Remote Enable is another bus management line which helps select between two alternate sources of programming data, i.e., front panel controls and GPIB.

EOI (End or Identify)

This bus management line indicates the end of multiple-byte transfers, or is used with ATN to perform a parallel polling sequence.

2.3.7.3 SYSTEM CONNECTION

Since the GPIB is designed for byte-serial, bit parallel operation, Models 7065 and 7075 equipped with Option P2 are programmed by a series of ASCII characters supplied by a bus controller. It is the combination of this controller and either model digital delay generator, with Option P2, which provides the mechanics for addressing, handshaking and data transfer. Connect the controller and instrument with an electrically compatible cable, such as an Amphenol Interface Bus Cable (assy. no. 408-30111-302). Then, select the appropriate device address making sure the rear-panel toggle switch is in the REM EN (Remote Enable) position.

NOTE: Conformance with the IEEE standard is important. Therefore, it is essential that all of the specifications stated on the interconnect cables be met!

Table 2-2. IEEE 488 GPIB P2 Connector Pin Assignments.

CONTACT NO.	SIGNAL LINE	CONTACT NO.	SIGNAL LINE
1	DI01	13	DI05
2	DI02	14	DI06
3	DI03	15	DI07
4	DI04	16	DI08
5	EOI	17	REN
6	DAV	18	Gnd. (6)
7	NRFD	19	Gnd. (7)
8	NDAC	20	Gnd. (8)
9	IFC	21	Gnd. (9)
10	SRQ	22	Gnd. (10)
11	ATN	23	Gnd. (11)
12	SHIELD	24	Gnd. LOGIC

NOTE: Gnd. (n) refers to the signal ground return of the referenced contact.

2.3.7.4 PROGRAMMING DATA

The Model 7065 and 7075 programming format consists of a series of ASCII characters (up to twelve) which select the memory address being used, the digit(s) to be changed, the new data, and the execute command. A total of sixteen memory addresses are available, each capable of storing one complete instrument setting consisting of the nine preset data digits. Any digit can be changed either individually or together in some appropriate combination.

The first character (P) designates the memory address to be changed. If the current memory address is suitable, this character does not have to be sent. Any of the sixteen available memory addresses is accessed directly by sending one of the sixteen consecutive ASCII characters starting with "P". These are listed in Table 2-3.

The IEEE-488 Bus

The IEEE Interface Bus transfers data and commands between the components of an instrumentation system on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cables connect all instruments, controllers, and other components of the system in parallel to the signal lines.

Eight of the lines (DIO1-DIO8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous, coordinated by the three handshake lines (DAV, NRFD, NDAC). The other five lines are for control of bus activity.

Devices connected to the bus may be talkers, listeners, or controllers. The controller dictates the role of each of the other devices by setting the ATN (attention) line true and sending talk or listen addresses on the data lines (D101-D108). Addresses are set into each device at the time of system configuration either by switches built into the device or by jumpers on a PC board. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers will be automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently.

The ATN line is one of the five control lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using the ASCII code*. When ATN is false, any code of 8 bits or less understood by both talker and listener(s) may be used.

The other control lines are IFC, REN, SRQ, EOI.

IFC (interface clear) places the interface system in a known quiescent state.

REN (remote enable) is used with other coded messages to select either local or remote control of each device.

Any active device can set the SRQ (service request) line true. This indicates to the controller that some device on the bus wants attention, say a counter that has just completed a time-interval measurement and wants to transmit the reading to a printer.

EOI (end or identify) is used by a device to indicate the end of a multiple-byte transfer sequence. When a controller sets both the ATN and EOI lines true, each device capable of a parallel poll indicates its current status on the DIO line assigned to it.

In the interest of cost-effectiveness it is not necessary for every device to be capable of responding to all the lines. Each can be designed to respond only to those lines that are pertinent to its function on the bus.

*American Standard Code for Information Interchange

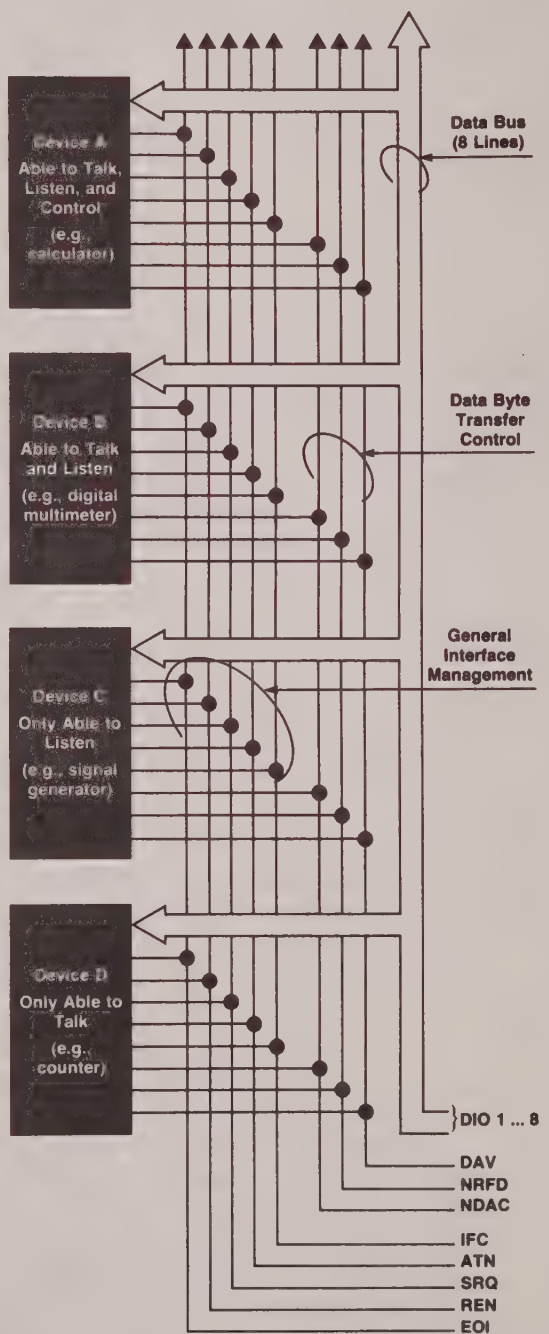


Figure 2-1. General Purpose Interface Bus (GPIB).

FORMAT: Typical examples of full instruction sequences which change the data in a chosen memory address is shown below:

Standard Instrument:	P	C	123456	!
Instrument with Option A:	P	@	123456789	!

Memory Address → Decade Selected → Numerical Data (Time Setting) → Execute

The next character of the format selects the specific location in the following field of nine locations where the next entry will go. This can be any digit in the format. This example starts at the beginning with the MSD, hence the "@". Additional changes can be made in succeeding locations of the field from which the initial change was made. If changes are in consecutive sequence then only the actual appropriate entries need be sent. If, however, you want to skip past one or more decade locations (which presumably already have correct entries in place), then you must first define the next location in the field with one of the ASCII characters "A" through "H" as set forth in Table 2-3. Any one of numerous characters may be used as the "execute" character and are listed, along with their bit patterns, in Table 2-4.

Here are some examples of typical messages:

1. Change all digits, enter a delay of 123456 ns (123456789 for Option A) and use memory "P". To accomplish this, use the entire field: the message is

   P C 123456 ! (with Option A, P @123456789 !).

   "P" corresponds to the memory being addressed. "C" corresponds to the 100 μs digit (the most significant digit to be changed), 123456... is the data entered while " ! " is the message-execute command. As soon as the instrument receives " ! ", it will begin generating a delay of 123456... ns.

2. Change the 1 μs digit from its present value to a value of 5 without changing memory. To make the change, the controller must send only three (3) characters: E 5 ! . The "E" addresses the 1 μs digit. The "5" enters the value and the " ! " causes the command execution.

3. Preload 11111 μs in memory register Q for use at a later time. To accomplish this function, a message similar to Example 1 is required (but without the " ! " which causes the execution): Q C 11111 . Memory Q will now have the value 11111 μs stored as delay setting.

Table 2-3. Digit and Memory Register Address Characters and Bit Patterns.

DESCRIPTION	ASCII CHAR	BIT PATTERN							
		b8	b7	b6	b5	b4	b3	b2	b1
100000000 (MSD)	@	X	1	0	0	0	0	0	0
010000000	A	X	1	0	0	0	0	0	1
001000000	B	X	1	0	0	0	0	1	0
000100000	C	X	1	0	0	0	0	1	1
000010000	D	X	1	0	0	0	1	0	0
000001000	E	X	1	0	0	0	1	0	1
000000100	F	X	1	0	0	0	1	1	0
000000010	G	X	1	0	0	0	1	1	1
000000001 (LSD)	H	X	1	0	0	1	0	0	0
MEM #0	P	X	1	0	1	0	0	0	0
1	Q	X	1	0	1	0	0	0	1
2	R	X	1	0	1	0	0	1	0
3	S	X	1	0	1	0	0	1	1
4	T	X	1	0	1	0	1	0	0
5	U	X	1	0	1	0	1	0	1
6	V	X	1	0	1	0	1	1	0
7	W	X	1	0	1	0	1	1	1
8	X	X	1	0	1	1	0	0	0
9	Y	X	1	0	1	1	0	0	1
A	Z	X	1	0	1	1	0	1	0
b	⊏	X	1	0	1	1	1	0	1
C	\	X	1	0	1	1	1	0	0
d	⊐	X	1	0	1	1	1	0	1
E	^	X	1	0	1	1	1	1	0
F	—	X	1	0	1	1	1	1	1

X = don't care

4. Execute the delay value stored in memory Q, Example 3. The memory Q is addressed and " ! " causes execution.

5. Change the 100 ns and 10 ns digits only. This change is accomplished by addressing the 100 ns digit, then sending two numbers: F 3 3 ! . Accordingly, the 100 ns decade is changed to 3, the 10 ns is also changed to 3 without changing any other digit, and without using the memory, i.e., if the setting is 111111 ns, the new delay after the message becomes 111331 ns.

Table 2-4. Characters and Bit Patterns Allowable for Execute Command. The Recommended Character for Use is " ! " .

ASCII CHAR	BIT PATTERN							
	b8	b7	b6	b5	b4	b3	b2	b1
SP	X	0	1	0	0	0	0	0
!	X	0	1	0	0	0	0	1
"	X	0	1	0	0	0	1	0
#	X	0	1	0	0	0	1	1
$	X	0	1	0	0	1	0	0
%	X	0	1	0	0	1	0	1
&	X	0	1	0	0	1	1	0
'	X	0	1	0	0	1	1	1
(	X	0	1	0	1	0	0	0
)	X	0	1	0	1	0	0	1
*	X	0	1	0	1	0	1	0
+	X	0	1	0	1	0	1	1
,	X	0	1	0	1	1	0	0
-	X	0	1	0	1	1	0	1
.	X	0	1	0	1	1	1	0
/	X	0	1	0	1	1	1	1

2.3.7.5 OPERATING CONSIDERATIONS AND VARIABLES WITH THE P2 OPTION

NOT USED FUNCTIONS -

When operated with the P2 Option, the Models 7065 and 7075 do not employ the full range of GPIB functions. As is the case with many GPIB-compatible instruments, the two units operate with a kind of 'subset' of functions within the broader IEEE standard. One reason this subset has been established is because the units are listen-only instruments and, therefore, are non-pollable. The EOI (End or Identify) line, for example, is not used because the line is a talker-response line. REN (Remote Enable) is not used because the instruments contain an internal address capability which performs essentially the same function. The D108, data bus message line is not used simply because the instruments do not need eight information sources.

SRQ LINE VARIABLES -

Ordinarily, the units operate with the SRQ line in the high, not active, state. The instrument is not requesting service. Conversely, in the low state, service is being requested. The controller senses one of the two states and acts accordingly, going into a pollable mode when it senses the low state.

Now, if the Error light comes on—usually meaning the trigger period is less than the delay—the SRQ line may be pulled low, or disabled, depending on the error-disable dip-switch setting on the instrument rear panel. When the switch is open (and the Error light is on), the line will go low. And the line will disable when the switch is closed.

Depending on the application or use of the instrument (e.g., kind of experiment being performed), an operator may or may not want to alter the signal state. Therefore, to provide the user with an option, and because an SRQ low level cannot be implemented as part of the IEEE standard, the error-disable switch (rear panel), if placed in the down (open) position, will permit the unit to put out a low-level signal. Otherwise, the SRQ line will not be exercised.

Other features of Option P2 that modify instrument operation, and are worth noting, are these:

A. If the instrument is triggered when data are being internally transferred as a result of a GPIB execute command, it means the programmed data in the instrument's shift registers will be accessed while data are being processed through them, thereby producing an erroneous delay/gate output. To avoid this problem, the instrument must not be triggered at the wrong time, i.e., during the interval of data transfer from memory to shift registers which takes place: coincident with a GPIB execute command and up to 10 μs thereafter. Or, the A and B RESET MODE switches can be used to retime the internal update to block an erroneous output as described later.

When the "A" switch is <u>off</u>, the circuits for retiming the reset pulse are inoperative and the instrument automatically updates itself with the beginning of each delayed pulse/gate output. Any new programming data from the GPIB fed in at the right time (outside the data transfer interval described above) will be entered into the appropriate circuit elements to produce the modified or new delay/gate time output upon the reception of the <u>second</u> input trigger. The first trigger will initiate one more output of the "old" time setting and the subsequent trigger the "new" time setting. The above is predicated on operation that withholds all triggering during the data transfer interval.

When the "A" switch is <u>on</u>, update timing is changed to provide either of two possible reset (update) modes depending on how the "B" switch is set.

1. When "B" is <u>off</u>, updating automatically takes place so that the next delay/gate output reflects the new time setting immediately. Again, however, triggering must be limited so as not to take place during the data transfer time defined earlier.

2. When "B" is <u>on</u>, the instrument's circuitry is latched to provide an expanded reset (update) period which occurs over the duration of the

Table 2-5. Listen Addresses.

DECIMAL ADDRESS	ASCII CHAR	BITS				
		b5	b4	b3	b2	b1
0	SP	0	0	0	0	0
1	!	0	0	0	0	1
2	"	0	0	0	1	0
3	#	0	0	0	1	1
4	$	0	0	1	0	0
5	%	0	0	1	0	1
6	&	0	0	1	1	0
7	'	0	0	1	1	1
8	(	0	1	0	0	0
9	)	0	1	0	0	1
10	*	0	1	0	1	0
11	+	0	1	0	1	1
12	,	0	1	1	0	0
13	-	0	1	1	0	1
14	.	0	1	1	1	0
15	/	0	1	1	1	1
16	0	1	0	0	0	0
17	1	1	0	0	0	1
18	2	1	0	0	1	0
19	3	1	0	0	1	1
20	4	1	0	1	0	0
21	5	1	0	1	0	1
22	6	1	0	1	1	0
23	7	1	0	1	1	1
24	8	1	1	0	0	0
25	9	1	1	0	0	1
26	:	1	1	0	1	0
27	;	1	1	0	1	1
28	<	1	1	1	0	0
29	=	1	1	1	0	1
30	>	1	1	1	1	0
Unlisten Command	?	1	1	1	1	1

b8 = don't care, b7 = 0, b6 = 1 NOTE: Valid only when ATN is True.

data transfer interval. This serves to inhibit the instrument from accepting triggers during the data transfer interval; therefore, the user need not be concerned with trigger timing to avoid possible erroneous outputs. Again, the next trigger (accepted) will cause the instrument to produce a delay and gate output of the new time setting.

B. If the rear panel toggle-switch is in the REM EN (Remote Enable) position, the units when powered up will automatically come up in the Local mode. The instruments will remain in this mode until they are addressed by the GPIB. They will then switch to the remote state and remain there until the rear panel is switched to LOC (Local Control) or until the power is switched off.

C. On power-up, the units automatically have memory "P" in use. If a memory change is unnecessary, the first character in a command message need not be used.

D. Models 7065 and 7075 accept all listener addresses except #32 which is the Unlisten address. These addresses are set in the units using five rear-panel switches. The ASCII address which corresponds to the address switch settings is shown in Table 2-5.

Note: These characters represent addresses only during the time ATN is asserted.

SECTION 3

DESIGN PRINCIPLES & CIRCUIT DESCRIPTION

3.1 GENERAL

The objectives of this section are to:

1. Familiarize a user or maintenance technician, working with the Model 7065 or 7075, with the purpose and function of the instruments' principal circuits.

2. Provide enough design details for each of the principal circuits so that a technician will understand the:
   a. interaction between major segments comprising various circuits
   b. operating characteristics and interfacing of the circuits
   c. routing and logic relationships of the input and output signals
   d. limitations of the operating modes.

3. Provide the relevant block and timing diagrams.

4. Supply the user and technician with sufficient circuit function and design detail to maintain, troubleshoot and repair an instrument with no or minimum assistance from the manufacturer. Test and calibration procedures are separately described in Sect. 4.

Figs. 3-1 and 3-2 illustrate in block diagram form the relationship between the principal circuits of the Model 7065 and 7075. Fig. 3-1 includes all of the major instrument sections from the power supplies, through the timing circuits to the output signals. The second figure, 3-2, is a detailed block diagram of specific timing circuit sections. The reader should become familiar with these diagrams as well as the waveshape diagrams and schematics and refer to them frequently to better understand the circuit relationships explained in the text. A clear overview of the signal routings and relationships is also important.

Figs. 3-3, 3-4 and 3-5 illustrate pulse timing at various test points (TP) on the identified circuit boards. The relationships shown are derived from a 123 ns digital time setting and apply as superimposed to a 1/4" grid where one horizontal division equals 10 ns.

3.2 CIRCUIT OPERATION AND FUNCTION

3.2.1 INTRODUCTION AND OVERVIEW

After power is applied to the instruments, the Input circuits generate an Oscillator Stop signal which is initiated in one of three ways: 1) by an external trigger introduced to the instrument through the trigger discriminator, 2) through a manual trigger generator, or 3) through an internal trigger generator (Model 7075 only).

The Oscillator Stop signal is sent to Clock Synchronizing circuits to control the oscillator which, in turn, provides a clock signal phased with the trigger signal. The clock and trigger are then sent to the Timing circuits.

These Timing circuits produce an Initial pulse which starts a countdown process through the delay setting circuitry to generate a Delayed pulse and a separate Gate pulse whose leading edge coincides with the leading edge of the initial output pulse while its trailing edge coincides with the leading edge of the delayed output. These relationships are shown in Fig. 3-2.

Settings made with the Thumbwheel switches select and indicate the desired number of nanosecond increments between the initial and delayed pulses. This data is processed by the Timing circuits to produce the Initial, Delayed and Gate pulse differential drive signals which are then introduced to output amplifiers. The amplifiers condition these differential signals to provide TTL and "quasi-" ECL outputs. (See also Para. 3.2.6.)

3.2.2 POWER SUPPLIES

AC line power (115/230 volt, 50/60 Hz) enters the instruments through a step-down transformer, then enters the ± 12 volt and ± 5 volt power supplies where it is converted to DC power.

Power for the ± 5 volt supplies is converted by an external rectifier unit, while the ± 12 volt supplies contain an internal rectifier. All instrument components are DC-powered except for the power ON/OFF switch, intake fan, overtemperature shutoff switch and fuse. Schematic 7065-39 shows the power supply interconnections.

3.2.3 INPUT CIRCUITS (Schematic 7065-30)

Fig. 3-1 shows the three principal circuits that comprise the Input circuits. These are the Input Trigger Discriminator, Manual Trigger Generator and Internal Trigger Generator. The latter circuit is exclusive to the Model 7075, while the other two circuits appear in both models. Model 7065 is triggered externally or manually. It has no internal triggering capability. But the Model 7075 is capable of triggering in three modes: External, Internal and Manual.

A. Input Trigger Discriminator

This circuit is a phase discriminator which converts the External Trigger Input signal (TTL) to an ECL signal thereby making the incoming signal acceptable and compatible to the instruments' internal control circuitry.

B. Manual Trigger Generator

This circuitry is common to both the Models 7065 and 7075 and is used to generate trigger signals during single-cycle operation. Its output signal is also converted to ECL form by the Input Trigger (phase) discriminator prior to entry into the Clock Synchronizing circuits.

C. Internal Trigger Generator

This generator, peculiar to the Model 7075 only, produces 5 Hz to 5 MHz trigger signals.

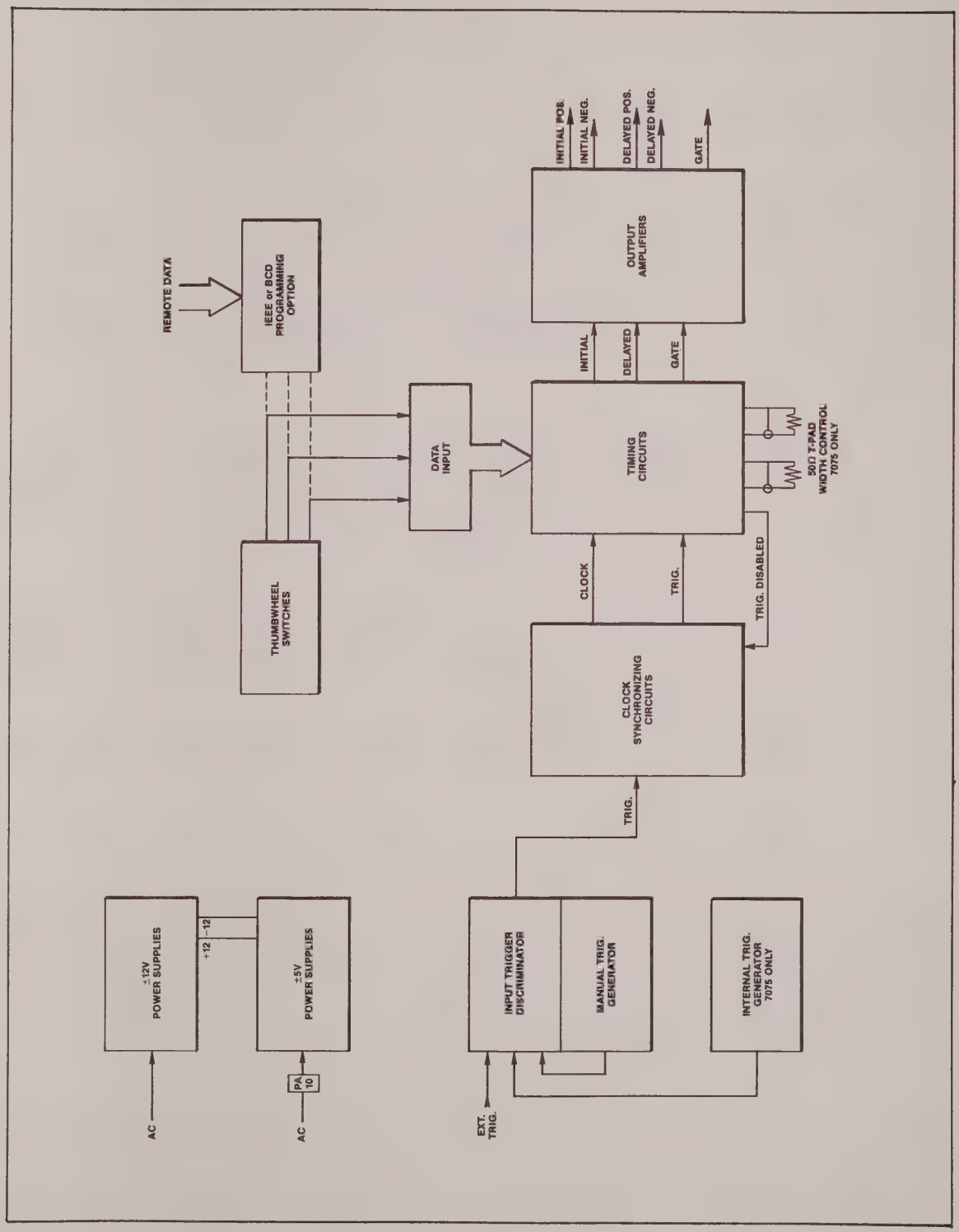


FIG. 3-1. Block Diagram showing the relationship between the major instrument sections from the power supplies through the timing circuits to the output signals.

As with the manually generated signals, these are also conditioned by the phase discriminator prior to use by the other instrument circuits.

The product of these input circuits is a Clock-Stop signal—the Input Discriminator output—which controls the operation of the Clock Synchronizing circuits.

3.2.4 CLOCK SYNCHRONIZING CIRCUITS (Schematics 7065-31, 7065-39, 7075-39)

These circuits consist of a counter, start oscillator, two phase detectors, a loop filter/amplifier and crystal oscillator. Together, the circuits constitute a master oscillator—which in this case functions as a master clock—for the instruments' Timing circuits. Specifically, the clock initiates the 100 MHz clock signal, while the overall function of the Clock Synchronizing circuits is to provide outputs which are time-coherent with the Input Trigger pulses (or Trigger Output, depending on the point of view).

The Clock-Stop signal from the Input Trigger Discriminator latches a one-shot. In turn, the one-shot stops the oscillator for a 28 ns delay, after which the oscillator is restarted. It is this delay/restart sequence that initiates a digital timing cycle. The delay procedure ensures that the start of the timing cycle is always synchronous with the trigger input pulse leading edge, by which any indeterminacy between the input trigger and start of the count signal is eliminated.

To maintain a stable 100 MHz frequency, and guarantee delay accuracy exceeding 1 ns, the (temperature compensated) clock oscillator is phase-locked to the temperature-stabilized crystal oscillator. Acting together, these design schemes form the heart of the Model 7065 and 7075 instruments, and produce unusually accurate jitter-free delays.

Now the clock and trigger outputs are synchronized, and are sent on to the Timing circuits (Para. 3.2.5).

3.2.5 TIMING CIRCUITS

These circuits comprise the digital mechanisms which produce the Initial, Gate and Delay pulses—the end-products, or outputs, of the 7065 and 7075 instruments. The period between the Initial pulse and Delay pulse establishes a time-interval (the magnitude being preset by the operator), which is measured in nanosecond increments. The Gate pulse provides an operator with a convenient "window" between the Initial and Delayed pulses, its width being determined by the leading edges of the two pulses. Although the Gate pulse is always triggered whenever the Initial and Delay pulses are triggered, it is not significant or accurate if its width is less than 10 ns.

The Timing circuits also produce a fourth signal, the Coincidence signal, which performs the actual Delayed pulse triggering function. Triggering occurs when the count from the 10 ns Decade counter reaches zero (0), or when the count is initially set at zero. In other words, the Coincidence signal is the mechanism which ensures that the Delayed pulse occurs precisely at the end (zero count) of the Initial/Delayed pulse interval.

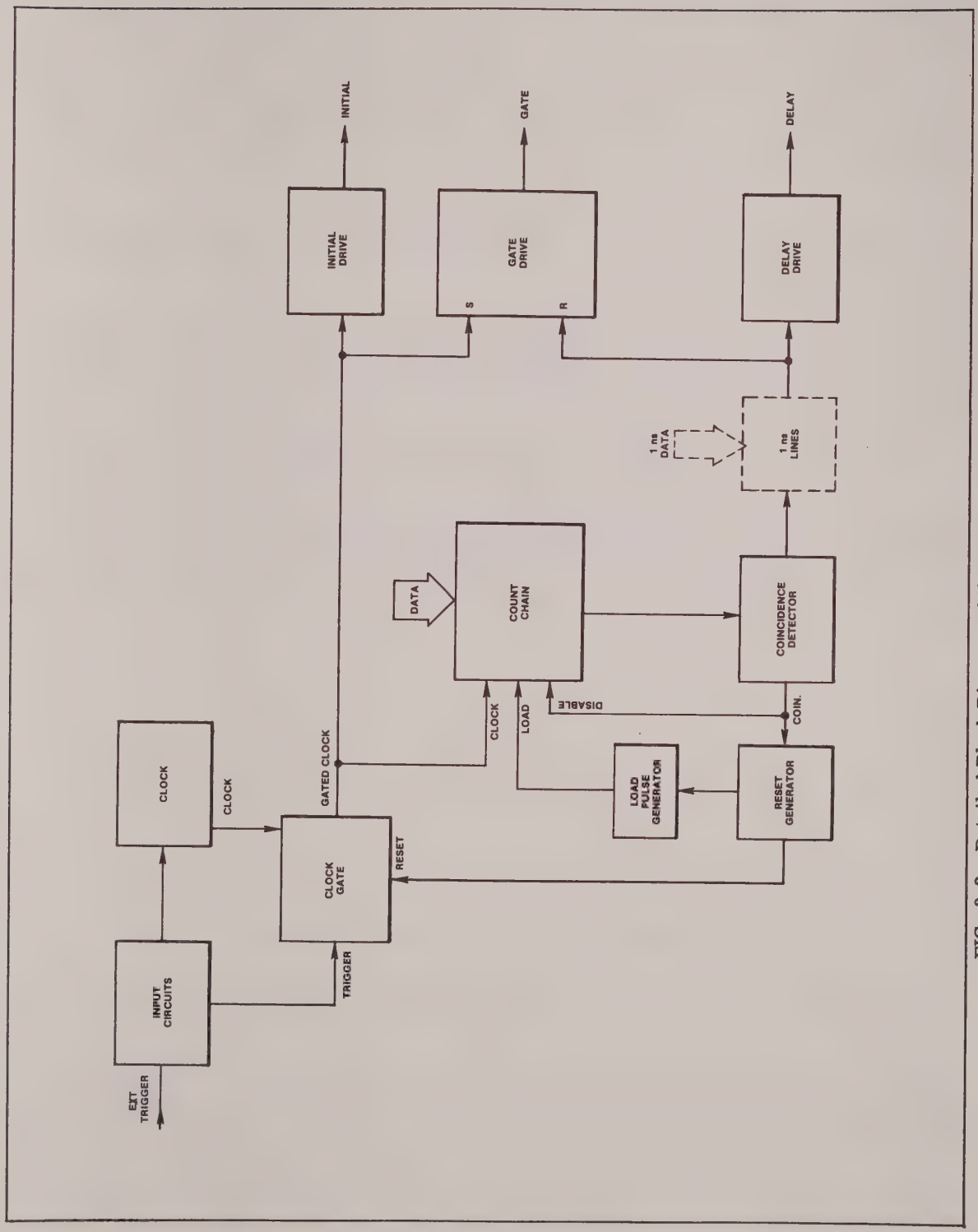


FIG. 3-2. Detailed Block Diagram of the specific timing circuit sections.

And finally, the Timing circuits generate a Trigger Disable signal which disables the trigger during the delay cycle.

From the Clock Synchronizing circuits, the first Clock pulse generates the Initial pulse and sets the beginning of the Gate pulse. The Delayed pulse is also established by the Clock pulse. However, the time at which it is actually triggered is determined by the number of 10 ns increments set into the count chain. In other words, the interval between the Initial and Delay pulses is the:

Delay Pulse (initiation) + "N" ns increments.

The settings are made either manually with the thumbwheel switches or automatically through the optional remote programming circuits.

The Initial/Delayed pulse interval also establishes the end of the Gate pulse. And included within the Timing circuits is a sub-circuit which permits a further breakdown of the 10 ns increments into 1 ns increments, thus, 1 ns resolution settings can be made.

The Timing circuits operate at both ECL and TTL levels. Those segments of the circuits directly affected by or related to the 100 MHz clock function are at ECL, because they must also operate at 100 MHz. The balance of the Timing circuits, essentially the Data Input circuitry, operates at TTL. Incidentally, the Coincidence signal also operates at both TTL and ECL levels. If the Initial/Delay pulse interval is greater than or equal to 100 ns, the signal operates in TTL. If the counting is done at less than 100 ns, the Coincidence signal operates in ECL. Although TTL is slower, it offers the advantage of simpler circuit design with lower power consumption.

3.2.6 OUTPUT AMPLIFIERS

Models 7065 and 7075 each contain three output amplifiers. Two of the amplifiers produce Initial and Delayed output pulses, while the third produces a Gate pulse output. Each amplifier accepts a complimentary (positive and negative) ECL-level input, and all three amplifiers are identical in design.

The principal function of these amplifiers is to:

1. Boost the power of the three pulses by increasing the voltage and current levels.

2. Translate, or condition, the ECL signals such that the outputs are suitable for other instruments operated with the delay generators.

A direct ECL output would be very sensitive to loading and short circuiting (an ECL gate might be damaged). Moreover, (as in the first function) without amplification and level translation, the TTL levels cannot be produced from an ECL gate.

Power is boosted from the ECL amplifier input of -0.7 volt to -1.7 volts, to an Initial and Delayed pulse output level of +5 volts into 50 ohms (Pos.) and -1 volt into 50 ohms (Neg.). The Gate pulse

output is boosted to +5 volts into 50 ohms. Although these output signals (being higher) are neither specifically ECL or TTL, they are kept characteristically similar to those levels. The amplifiers' design concept necessarily allows for the fact that some instruments, used in association with the 7065 and 7075, only accept TTL. Others trigger only with ECL. And still other instruments accept either ECL or TTL, and trigger on either the positive or negative pulse slope. Thus a user may want the availability of two outputs coincident with the same event.

A final and important feature of the Models 7065 and 7075 is that the outputs are short-circuit protected to prevent the output stage from being damaged if it is shorted out to ground. Thus, if the amplifier output is grounded, the current through the output is limited.

The Model 7075 has an additional capability making it distinctive from the Model 7065. A Tee-pad (attenuator), placed between the amplifier and output signal, permits continuously variable control of the positive Initial and Delayed pulse signal amplitudes. Some instruments, used in conjunction with the 7075, might not trigger or might double-trigger in response to the delay generator's typical TTL-type signal. The Tee-pad allows for a decrease in the output amplitude to make the 7075 more compatible with the sensitivity of associated instruments.

The Initial and Delayed widths and the positive amplitudes can be set with the Model 7075. The fixed GATE OUT amplitude has a width equal to the time between the initial and delayed pulses. The Model 7065's output pulses are fixed while the 7075's pulses can be varied from 15 ns to 1 μs by using the Width control on the front panel.

3.3 CIRCUIT DESCRIPTIONS

3.3.1 POWER SUPPLIES

The BNC Models 7065 and 7075 use the following regulated power supplies:

Qty.	Voltage
2 ea.	+12 volt supplies
2 ea.	-12 volt supplies
2 ea.	+5 volt supplies
2 ea.	-5.2 volt supplies

Each supply operates in a similar manner. Therefore, in the following description, the +12 volt power supply operating characteristics are used as a model (except where noted).

AC-voltage from the transformer (T1) secondary coil is full-wave rectified by diodes CR1 and CR2 and filtered by the capacitor C1. Z1 is a three-terminal positive regulator which produces a regulated voltage output up to a current level of 1.5 amps. The output voltage is adjusted at the reference terminal, while the voltage level at the output is kept at +5 volts with reference to the terminal.

Operational amplifier Z2D senses approximately one-half the regulated output voltage at its inverting input. An adjustment potentiometer, R3, is located at pin 13 (Z2D). The output voltage is compared to a reference voltage from Zener diode CR5, and an error voltage is produced at the regulator's reference terminal. Thus, the nominal voltage at the reference terminal is +7 volts (5 volts below the output). Zener diode CR6 limits the reference to a level below 9.1 volts to prevent the regulated output from exceeding approximately 14 volts, thereby avoiding damage to the circuit elements in the load.

The +12(B) regulator circuit also uses the same voltage reference from Zener diode CR5, although it is non-adjustable. The -12 volt regulators, however, are referenced to the +12 volt (A) output.

Five-volt regulator circuits use the 12-volt (A) outputs for operating supplies, as well as reference supplies. Therefore, any failure of the plus (+) or minus (-) 12-volt (A) supplies also affects the 5-volt regulators. Operation of these regulators is otherwise identical to that of the 12-volt regulators.

The two primary windings on transformer T1—normally connected in parallel for 115-volt operation—may be connected in series for 230-volt operation by means of the rear panel slide-switch S901. If the temperature in the unit exceeds 60^{O} C, thermal cutout switch S903 will open, break the primary circuit, and shut down the unit.

3.3.2 INPUT CIRCUITS (Schematic 7065-30)

The input circuits for both the Model 7065 and 7075 are essentially the same. Both schematic drawings contain the same information.* The exception is the Internal Trigger Generator circuit shown on the lower left-hand quadrant of Schematic 7065-30. In the following circuit analysis and description, the reader should keep in mind that references to the Internal Trigger Generator apply to the Model 7075 only.

3.3.2.1 EXTERNAL TRIGGER CIRCUIT

This circuit is shown in the upper right-hand quadrant of the schematic. Within the circuit is comparator Z7, which is enabled by its pin 4. When Z4 is in the enabled state, the External Input Trigger enters the circuit at J801 where it is attenuated by resistors R68, R69 and R70. These resistors also protect the comparator against damage from overvoltage, while feedback resistor R74 protects against multiple-triggering by generating hysteresis.

Potentiometer R801 permits selection of the input signal DC-level at which the comparator triggers. The potentiometer adjusts the comparison level of the inverting input at pin 3, Z7, and thus adjusts the voltage at which the comparator switches. Complimentary outputs from pins 7 and 8, Z7, drive NOR gates Z8B and Z8A respectively. One of the signals, going to each gate, is delayed by an RC-network comprised of either R81/C29 or R79/C28. This interconnection scheme permits the gating circuit to differentiate between the positive and negative edge of the incoming signal.

*Both models are shown on Schematic Diagram 7065-30.

When the slope switch, S801, is in the plus (+) position, the anode of diode CR11 is grounded. Thus, pin 9 of Z8B is at a high ECL level and the gate is disabled. At the same time, CR12 is reverse-biased and Z8A is enabled. Conversely, for negative slope selection, Z8A is disabled while Z8B is enabled.

Outputs from the Z8A and Z8B ECL gates are connected with the output of NOR gate Z3A in a wire-ORed (i.e., parallel-gated) arrangement. The combined output of these three gates is the Oscillator Stop signal.

As previously described, when the 7065 or 7075 are externally triggered, gates Z8A and Z8B are enabled and disabled depending on the position of slope switch S801. However, when the instruments are in the Manual or Internal modes (internal for the 7075, only), the trigger comparator is disabled and NOR gate Z3A processes the Clock Stop (oscillator) signal.

On the Model 7075, with the Trigger Mode switch in the manual or external trigger position, pin 10 on inverter Z22B is pulled low through resistor R59. Pin 9 is connected to VBB, the ECL threshold voltage at pin 11, resulting in a high level at the comparator's pin 6. In turn, pins 3 and 5 are pulled high, thus disabling the internal trigger generator.

When one of the six internal trigger positions of S803 is selected, Z22B is clamped to a high ECL level by diode CR802. The wired-OR outputs, pins 3 and 5 on Z22A and Z22B respectively, are free to follow the level set by the Z22A input pins which are, in effect, an RC network selected by the frequency switch.

On the Model 7065, there isn't any internal trigger generator. Therefore, the trigger comparator is always enabled to act in the external trigger position and the manual trigger generator is also always enabled.

3.3.2.2 MANUAL TRIGGER GENERATOR

This circuit, shown on the left-hand side of the schematic, is enabled by a high ECL level at the common side of switch S802. Again, the high level is provided by the diode, CR802.

Gates Z2A and Z2B are combined to form an RS flip-flop debouncing circuit which changes state each time the manual pushbutton, S802, is depressed. Outputs from the flip-flop Z2A, Z2B are fed to NOR gate Z2D after being differentiated by NOR gate Z2C, R55 and C22. Gate Z2D's output is connected to the error detection circuitry at gate Z4B, pin 10, and gate Z3A, pin 4. The output, produced by wire-ORed gates Z3A, Z8A and Z8B, is the oscillator stop signal sent to the Clock Synchronizing circuits.

3.3.2.3 ERROR DETECTION CIRCUITS

When a timing cycle is in progress, the high-level signal at the trigger disabling gate (Z19A, Schematic 7065-32)—a product of the Timing circuits—is inverted by gate Z3B thus enabling gates Z4A,

Z4B and Z4C. Moreover, when the slope switch S801 is in the plus (+) position, diode CR10 keeps pin 4, Z4A, at an ECL high level thereby disabling the gate. As this occurs, Z4C is enabled. Conversely, if S801 is in the minus (–) position, Z4A is enabled and Z4C is disabled.

The inputs to these gates are the differential outputs of the external trigger comparator, Z7, differentiated by R84, C32 and R86, C33. Accordingly, the input to gate Z4B is the output of gate Z2D which NORs the internal trigger generator and manual trigger generator outputs. Wire-ORed outputs from gates Z4A, Z4B and Z4C are fed to the input of one-shot flip-flop Z3C, Z3D. If a trigger signal occurs while the trigger disable gate is high, (i.e., the gates are enabled), the resultant high-going pulse at pin 10, Z3C, fires a one-shot. The one-shot's low level output turns on transistor Q6 which subsequently supplies current to turn on the front panel Error light, LED DS801. Voltage from the DS801 anode is also sent to the IEEE programming circuits to provide an error signal on GPIB SRQ line.

3.3.3 CLOCK SYNCHRONIZING CIRCUITS (Schematic 7065-31)

When power is applied to the instrument circuits, provided none of the three trigger modes are activated, the Start Oscillator remains in a steady state while producing a 100 MHz Clock signal which goes to the Timing circuits. An ovenized crystal oscillator, operating at 101 MHz, is used as a highly stable reference for the Clock (VCO) frequency. The 1 MHz difference between the Clock signal and the crystal oscillator is stabilized by the operation of the First and Second Phase Detectors.

However, when a trigger mode is activated and a pulse is sent to and received by the Input circuits, a narrow Clock Stop pulse sets the Clock Stop flip-flop and the Start Oscillator is shut off. Then, after a 28 ns delay, the Clock Start signal is generated and the oscillator is restarted. This oscillator signal also initiates the Trigger Output signal.

NOTE

There is a time interval between the clock-restart and arrival of the trigger pulse, but this interval varies no more than ±50 picoseconds.

At the time the Start Oscillator is turned off, the two phase detectors and the counters are reset. The detectors are now in a known steady state, ready to resume their monitoring function when the Start Oscillator is again turned on. And when that event occurs, the First Phase Detector (actually a type of harmonic mixer) resumes its frequency comparison function.

The First Phase Detector's initial output occurs when the phases of the 100 MHz and 101 MHz frequencies are identical. Until that happens, the Divide-by-100 Counter (the two Divide-by-10 Counters, Z10 and Z21) is prevented from operating by the Holdoff circuits. These circuits sense the first transition and allow the Divide-by-100 counter to start. The time interval between pulse-triggering and

release of the counter may vary anywhere between 100 ns and 1000 ns depending on the relative phase difference of the two oscillators at the time of triggering. This interval can differ each time the instrument is triggered.

After the initial output, the First Phase Detector continues to function at an output rate of 1 MHz. At the same time, the Second Phase Detector compares the 1 MHz error signal to the 1 MHz signal which has been divided down from the 100 MHz Start Oscillator output. This second detector is a standard digital phase detector scheme applied to ECL, which employs NOR logic instead of the more common NAND logic found in TTL circuits. ECL/NOR logic is used because the Model 7065 and 7075 design parameters dictate high-speed operation coupled with precise stability requirements. By integrating the Second Phase Detector's error-correction signal with the correction signal fed back to the Start Oscillator, the loop is closed.

When the Clock Synchronizing circuits are in the steady state, any frequency deviation between the Crystal Oscillator and the Start Oscillator is sensed by the First Phase Detector and produces a deviation in its 1 MHz output. The Second Phase Detector then senses the aberration and generates an error signal which is amplified and fed back to the Start Oscillator to correct for the error condition.

Since only small corrections are made at each comparison, the steady state condition is not reached unless the time between trigger pulses is approximately 30 μs. But if the time is less, full corrections are made. Finally, when the Clock Start/Stop Oscillator is in phase with the Input Trigger, both signals are sent to the Timing circuits.

3.3.4 TIMING CIRCUITS (See Figs. 3-3 and 3-4, pages 3-13 and 3-17.)

3.3.4.1 CLOCK GATE

Before the trigger signal enters the Timing circuits—assuming no timing cycle is in progress—the signal level at TP-E, pin 5 of Z14A, is high, thereby preventing the clock at pin 4 from passing through the gate. However, when the timing trigger is introduced, the state of the set/reset flip-flop, formed by Z19B and Z19C, changes and causes the level at TP-E to go low. Now the clock can pass through gate Z14A.

At the end of each timing cycle, the reset circuitry generates a reset pulse at pin 9, Z19B, which resets the clock gate. Again TP-E goes high and the clock is inhibited from passing gate Z14A. The resultant signal is a gated clock at TP-D. (The total number of gated clock pulses is N plus 2 (N+2), where N represents the number of 10 nanosecond increments programmed into the instrument.)

3.3.4.2 TRIGGER DISABLE

Gate Z19A ORs the complement of the clock gate at TP-E with the reset pulse from gate Z14B, thereby causing a high disable signal whenever any timing cycle is in progress. This signal is sent to the input circuits for input error detection.

3.3.4.3 PULSE SET SIGNAL

When the clock gate is opened by the timing trigger, the first cycle of the gated clock passes through gate Z15B to the test point TP-F. At this test point, the high-rising pulse activates the set/reset flip-flop (Gates Z20B and Z20C) which returns the high signal to pin 9, Z15B, and blocks other clock pulses from passing the gate. At the end of the timing cycle, the flip-flop is reset by a reset signal emitted by pin 9 and Z20D. The resultant single pulse at TP-F is delayed by the four gates in the Z21 circuit.

Note that the number of gates in the pulse-set path is equivalent to the number in the pulse-reset path. The purpose of this scheme is to reduce temperature effects and equalize signal-propagation delays. The inverting input of comparator Z21 is connected to a reference voltage which can be varied to alter the switching points of the gates. It is this arrangement that provides for a small adjustment range in the timing of the pulse-set signal at TP-H, which brings the initial and delayed pulses into perfect coincidence at zero delay.

Transformation of the voltage change into a delay change occurs because the slope of an ECL signal is approximately three volts per nanosecond. Any level shift, therefore, results in a corresponding change in the timing signal. Comparison voltage is attained by buffering the VBB output of Z21 with the unity-gain operational amplifier, Z25A. Resistors R104, R81 and R80 then move the level slightly.

3.3.4.4 ECL COUNTER

The ECL Counter, Z12, counts down from the number programmed by the 10 ns data generated by either the thumbwheel settings or by the remote programming circuits. At pin 13, Z12, the clock input taken from gate Z14C ORs the complementary signal from the gate's clock with a signal from the reset circuitry. This switching procedure is necessary because the ECL Counter requires a clock transition during the time it is loaded. Because the ECL Counter outputs 00 through 04 are connected in a wire-ORed arrangement (i.e., counter outputs are all connected in parallel) an ECL low level occurs only when zero is reached. At which point, all the outputs are zero. This combined signal from pins 2, 3, 14, and 15, of Z12, is the ECL coincidence signal which drives the end of the count gate and TTL clock shaper. During the reset cycle, the combination of the low-level at pin 9, Z12, and a positive clock transition at pin 13 activates new data-loading into the ECL counter.

3.3.4.5 TTL CLOCK SHAPER

When the ECL coincidence signal is re-synchronized to the gated clock by NOR gate Z15C, translator Z13A shifts the gate output from an ECL to TTL level, and also serves as a one-shot. Its purpose is to widen the 10 ns pulses from the ECL counter to 35-ns wide TTL clock pulses required by the TTL circuits.

3.3.4.6 END-OF-COUNT GATE

Z15A, a three input NOR gate, acts as the end-of-count detector. The three input signals are an ECL

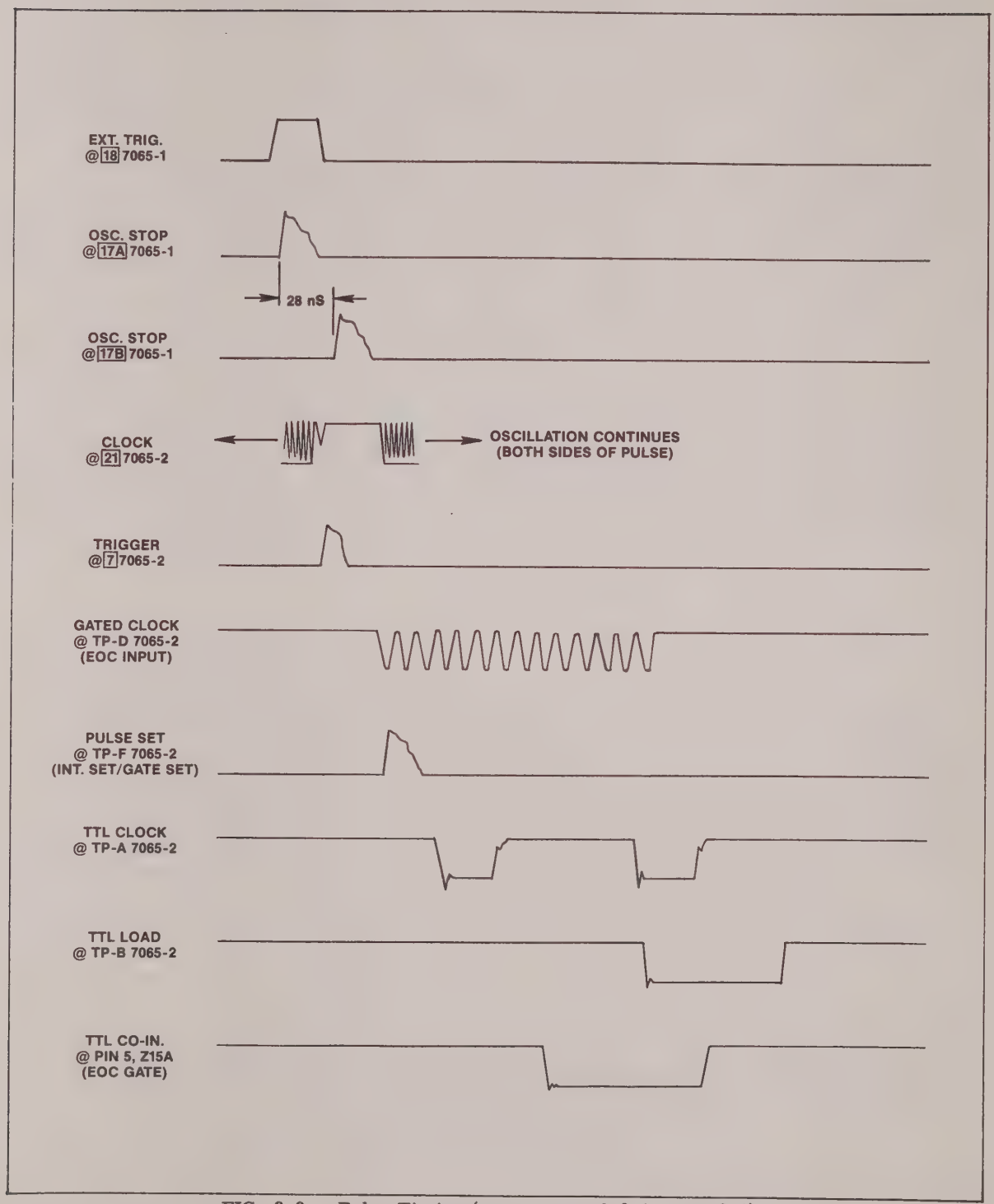


FIG. 3-3. Pulse Timing (see paragraph 3.1, page 3-1).
Additional timing diagrams in Fig. 3-4 on page 3-17.

coincidence, a TTL coincidence and a gated clock. All of these inputs must be low in order to produce a high output at the TP-G test point.

When the ECL counter reaches a count of zero, its wired-OR output goes low and thus indicates ECL coincidence. If the TTL counters have also reached zero, the TTL coincidence signal at TP-C is also low. The next low-gated clock cycle is then passed to test point TP-G. At the same time, gate Z14C passes the compliment of the gated clock cycle to the ECL counter, Z12. This counter then changes from zero count to the count of nine. The result is that the ECL coincidence signal returns high, thus preventing any further clocks from passing TP-G while a single, high-rising end-of-count pulse appears at TP-G. This latter pulse can be correctly called the pulse reset signal, since it resets the gate and provides a delayed pulse.

If ECL coincidence is reached, but the TTL counters have not reached zero, the TTL coincidence signal at TP-C will be high thereby disabling the end-of-count gate. In this event, the ECL counter continues counting and generates an ECL coincidence count at every tenth count. The coincidence signal shaped by the TTL clock shaper will clock the TTL counters until zero count is reached. At which time, the TTL signal will go low and stay low. While the ECL counter continues to count down from its preset value to zero, the subsequent ECL coincidence will generate an end-of-count pulse. Resistors R36 through R38 translate the TTL coincidence signal from ECL to TTL levels.

3.3.4.7 RESET CIRCUITS

The reset one-shot formed by gates Z20D and Z20A, at delay line DL6, is triggered by the end-of-count pulse at TP-G. Gate Z14B ORs the one-shot's undelayed output at pin 10, Z14B with a delayed output at pin 11. Meanwhile, the delayed output simultaneously passes gate Z14C and goes to the clock input of the ECL counter. Resolt: A positive transition occurs on the ECL counter's clock while the load input at pin 9 is held low. As previously noted, this scheme provides the necessary gating procedure to load new data into the counter. The complement of the ECL load pulse is applied to pin 9, Z19B, thereby resetting the clock gate. This pulse causes the level at TP-E to return high, and blocks further clock pulses from passing gate Z14A. A randomly occurring remote reset signal from the programming circuits can also trigger the reset circuit. The signal, translated from TTL to ECL levels by positive components, is buffered by gate Z16C to the Reset one-shot.

3.3.4.8 TTL LOAD SHAPER

Translator Z13B shifts the ECL load pulse compliment from ECL to TTL levels by translator Z13B. This NOT gate performs a double role by also serving as a one-shot to widen the low pulse to roughly 40 ns. As a result, the TTL load pulse is applied to each of the TTL counters to load new data to the next timing cycle.

3.3.4.9 ONE-NANOSECOND LINES

At TP-G, the end-of-count signal or the pulse reset signal buffered by gate Z16B, drive the Width 1 ns

lines. The non-inverting output signal from Z16B, pin 7, takes two paths. The first path is to gate Z17B and is undelayed, while the second path is delayed by 1 ns and drives Z17A. These two pulse output signals are wire-ORed to provide no incremental delay when Z17A is selected.

A description of the selection process follows:

The wire-ORed output drives two paths. The first is a delayed path to Z17C. The second is a 2 ns delayed path to Z17B. When Z17C is selected, no incremental delay is added. But when Z17B is selected, a 2 ns delay is added. Again, the outputs of these two gates are wire-ORed to provide the drive for the next stage. In a like manner, Gates Z18A and Z18D are used to select a 4 ns incremental delay. Z18B and Z18C are used to select the second 2 ns incremental delay. The output of the last two gates is combined to provide the pulse reset signal at TP-J. A similar selection process is employed for each delay line so that only the 1 ns line selection procedure need be described in detail.

The inverting inputs of Z17A and Z17D are held either at an ECL high level (to disable), or at a level close to the -1.3 volt (VBB) center of the ECL logic range (to enable). At gate Z17A (which selects the 1 ns line), the level at the inverting input is adjustable over a narrow range so that the delay can be precisely set to 1 ns. The 1 ns adjust trimmer, R82, is used for this purpose. It modifies the buffered VBB reference voltage provided by the unity-gain operational amplifier Z24D. In a similar manner, the precise delay of each of the other delay lines is set by using their respective adjustment trimmers.

Drive signals that select the delay lines are derived from ECL-type emitter follower outputs from Z10. When a high level is required to disable a gate, the emitter follower can easily drive the resistor from buffered VBB to pull the level to ECL high. However, when a gate is to be selected, the emitter followers try to drive the level to ECL low but are unable to do so, because the most negative voltage is close to VBB. The resultant signal is a back-biased emitter follower output and the selected gate input is allowed to stay close to the VBB level. Selection/Disable functions occur in pairs—each time a gate is selected another is disabled. For example, when Z17A is enabled, Z17B is disabled. This procedure is predictable because all selection signals arrive in pairs (e.g., Delay-line one and its complement).

The pulse-reset signal at TP-J is applied to the reset input of the gate pulse flip-flop, and is also applied to a one-shot formed by gates Z23C and Z23B. These gates produce the differential delay pulse sent to the amplifier circuits for amplification.

NOTE

Timing of the pulse-reset and end-of-delay signal is dependent on the programming of the Width 1 ns lines. The end-of-count programmer—since it precedes the Width 1 ns lines—depends only on the counted portion of the timing cycle.

3.3.4.10 GATE PULSE

Gates Z23A and Z22C form the set-reset gate pulse flip-flop. The pulse set signal at TP-H sets the flip-flop which is reset by a pulse reset signal at TP-J. Then, via a twisted-pair transmission line, the resultant gate pulse is sent to the amplifier circuits.

3.3.5 OUTPUT AMPLIFIERS

NOTE

The following discussion of the Initial Pulse Amplifier operation may be used as a model for both Delayed Pulse and Gate Amplifier operation.

The differential Initial drive pulse is received from the Timing circuits through twisted-pair transmission lines. A differential amplifier formed by Q1-Q2 amplifies the ECL level signal, while Q1 and Q2 collector signals drive a second differential amplifier, Q3-Q4.

The collector signal from Q3 becomes the positive Initial output pulse by driving emitter followers, Q5 and Q6. Diodes CR1 and CR2 minimize temperature effects by offsetting the base-emitter voltage drops across Q5 and Q6.

MODEL 7075 ONLY - INITIAL AND DELAYED PULSE

R803 is a balanced, 50-ohm tee-pad which provides a balanced 50-ohm load to the output amplifier, while it also allows the pulse amplitude to vary between near zero volts and full voltage. The Gate output has no attenuator output.

The pulse may be varied from 15 ns to 1 μs using the two control knobs on the front panel; one is for Initial Pulse width adjustment, the other for Delayed Pulse. The Initial Pulse Width control (left-hand side) varies the INITIAL POS and NEG widths simultaneously. The Delayed Pulse Width adjustment (right-hand side) simultaneously varies the DELAYED POS and NEG widths.

Transistor Q6 derives its steady-state collector current from transistor Q19. In turn, Q3 provides short-circuit protection for the output device. Since Q19's base-emitter is prevented from dropping below 6.9 volts, by Zener diode CR10, the maximum voltage drop across resistor R56 is limited to roughly 4.5 volts. And because all of the current to Q6 must pass through R56, the output current is limited, thus preventing damage to the device if a short-circuit or other overload condition occurs at the output.

GATE AMPLIFIER

The steady-state collector current of transistor Q18 is derived from transistor Q21. Transistor Q15, in turn, provides short-circuit protection for the output device. Since Q21's base-emitter is prevented from dropping below 6.9 volts by Zener diode CR12, the maximum voltage drop across resistor R60 is limited to roughly 4.5 volts. Moreover, because all of the current to Q18 must pass through R60, the output current is limited. Thus, damage to the device is prevented if a short-circuit or other over-voltage condition occurs at the output.

lines. The non-inverting output signal from Z16B, pin 7, takes two paths. The first path is to gate Z17B and is undelayed, while the second path is delayed by 1 ns and drives Z17A. These two pulse output signals are wire-ORed to provide no incremental delay when Z17A is selected.

A description of the selection process follows:

The wire-ORed output drives two paths. The first is a delayed path to Z17C. The second is a 2 ns delayed path to Z17B. When Z17C is selected, no incremental delay is added. But when Z17B is selected, a 2 ns delay is added. Again, the outputs of these two gates are wire-ORed to provide the drive for the next stage. In a like manner, Gates Z18A and Z18D are used to select a 4 ns incremental delay. Z18B and Z18C are used to select the second 2 ns incremental delay. The output of the last two gates is combined to provide the pulse reset signal at TP-J. A similar selection process is employed for each delay line so that only the 1 ns line selection procedure need be described in detail.

The inverting inputs of Z17A and Z17D are held either at an ECL high level (to disable), or at a level close to the -1.3 volt (VBB) center of the ECL logic range (to enable). At gate Z17A (which selects the 1 ns line), the level at the inverting input is adjustable over a narrow range so that the delay can be precisely set to 1 ns. The 1 ns adjust trimmer, R82, is used for this purpose. It modifies the buffered VBB reference voltage provided by the unity-gain operational amplifier Z24D. In a similar manner, the precise delay of each of the other delay lines is set by using their respective adjustment trimmers.

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NOTE

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3.3.5 OUTPUT AMPLIFIERS

NOTE

The following discussion of the Initial Pulse Amplifier operation may be used as a model for both Delayed Pulse and Gate Amplifier operation.

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The collector signal from Q3 becomes the positive Initial output pulse by driving emitter followers, Q5 and Q6. Diodes CR1 and CR2 minimize temperature effects by offsetting the base-emitter voltage drops across Q5 and Q6.

MODEL 7075 ONLY - INITIAL AND DELAYED PULSE

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The pulse may be varied from 15 ns to 1 μs using the two control knobs on the front panel; one is for Initial Pulse width adjustment, the other for Delayed Pulse. The Initial Pulse Width control (left-hand side) varies the INITIAL POS and NEG widths simultaneously. The Delayed Pulse Width adjustment (right-hand side) simultaneously varies the DELAYED POS and NEG widths.

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GATE AMPLIFIER

The steady-state collector current of transistor Q18 is derived from transistor Q21. Transistor Q15, in turn, provides short-circuit protection for the output device. Since Q21's base-emitter is prevented from dropping below 6.9 volts by Zener diode CR12, the maximum voltage drop across resistor R60 is limited to roughly 4.5 volts. Moreover, because all of the current to Q18 must pass through R60, the output current is limited. Thus, damage to the device is prevented if a short-circuit or other over-voltage condition occurs at the output.

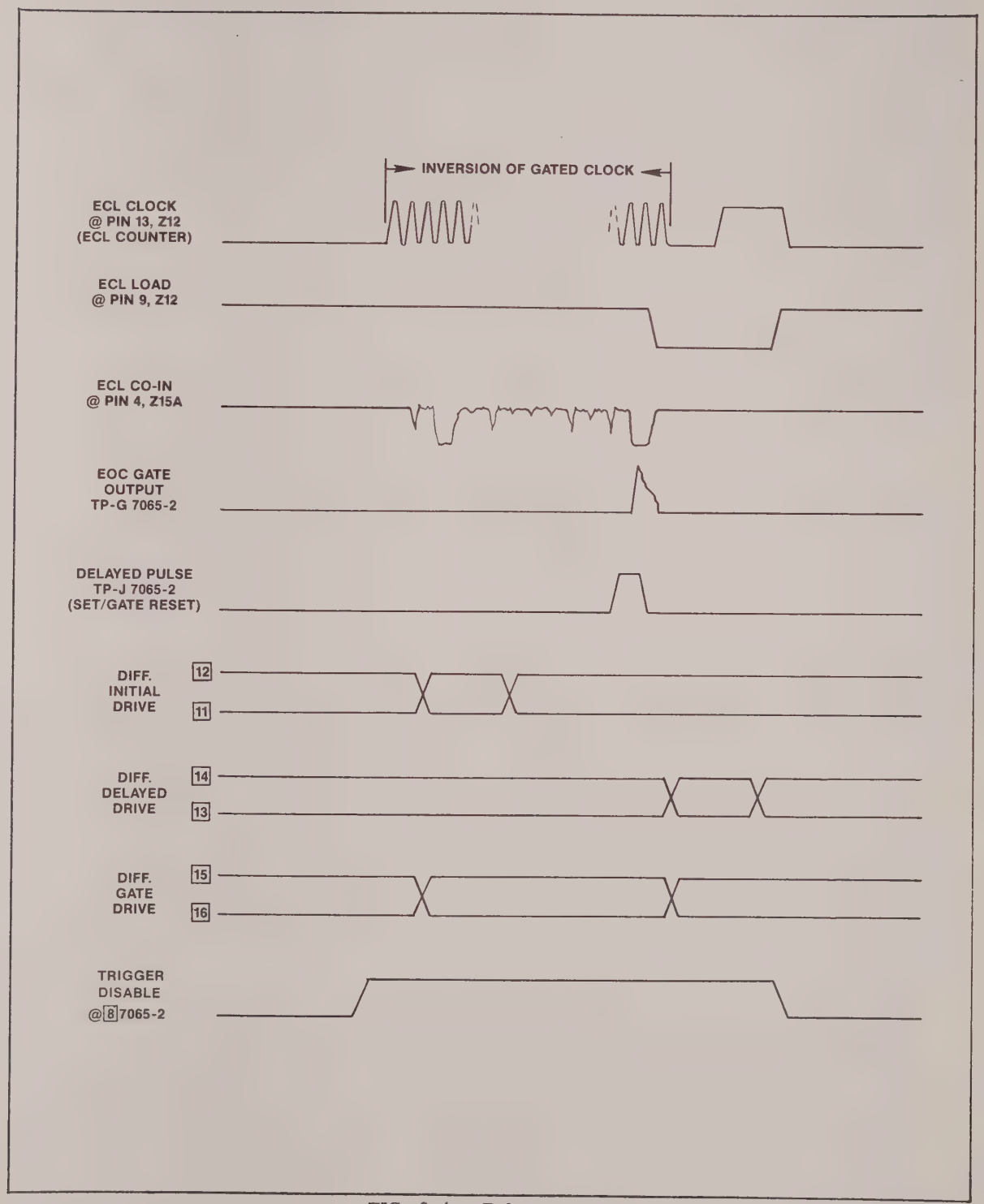


FIG. 3-4. Pulse Timing.

3.3.6 IEEE INTERFACE CIRCUITS - GPIB REMOTE PROGRAMMING - OPTION P2

3.3.6.1 INTRODUCTION AND NOTE TO THE READER

The IEEE Interface circuits permit operation of the Models 7065 and 7075 automatically in association with the General Purpose Interface Bus (GPIB). And although the circuits permit the instruments to be used in either a Local or Remote mode—for user flexibility and convenience—the real intent of the sophisticated circuit design is for remote operation. Actually, less than half the total circuit parts are used in the Local mode—namely, the Shift Registers. For this reason, the bulk of the text is devoted to an analysis of the Remote mode function.

Because many parts of the IEEE circuits operate simultaneously, a step-by-step signal trace or sequential description of the part functions is difficult. Thus, the reader will find some duplication and overlap throughout the following text.

NOTE

At the beginning of each cycle description (Address Cycle, Memory Select, etc.) is a list. These lists are the sequences in which information is outputted onto the Common Bus and distributed to the RAM or other parts of the circuits. The accompanying text provides a more detailed description of these sequences, but does not necessarily follow the same order.

3.3.6.2 DATA SIGNAL PROCESSING AND PROCESSING COMPONENTS

A. SHIFT REGISTER FUNCTIONS

The Models 7065 and 7075 IEEE Interface Circuits incorporate four shift registers (S/R), Z7 through Z10 on the schematic. These devices process information for the Timing circuits in either one of two instrument operating modes: Local or Remote. In the Local mode, data is shifted between the J1 through J3 inputs and the J11 through J13 outputs in a parallel-to-parallel fashion. During the Remote mode, information is transferred in a digit-serial, bit-parallel manner from the J (true) and $\overline{K}$ (complement) inputs to the Q-outputs and thus the J11 through J13 outputs.

B. LOCAL AND REMOTE DATA ENTRY

Local Mode:

Data are entered directly from the thumbwheel switch settings to the shift registers in the Local mode. No data are entered via the RAM bus, RAM or their associated circuits. The parallel inputs are tied directly to the thumbwheel switch inputs. Parallel loading from J1-J3 is accomplished at points A through H. The J11-J13 outputs appear at QA through QH. In this mode the clock is allowed to run freely to assure that the S/R outputs reflect the thumbwheel switch settings within a clock period time of 1 microsecond.

Remote Mode:

Whenever either of the delay generators is operated in the Remote mode, data are sent to the interface circuits from one or more of the seven IEEE Bus data lines, DIO-1 through DIO-7.

In the Remote mode, parallel loading of the S/Rs, Z7-Z10, is disabled and the registers are serially loaded from the RAM. Data, management and control messages are transferred from the GPIBs DIO-1 through -7 (-8 is not used) lines into the RAM circuitry, then to the S/Rs where the data signals are shifted and sent on to the counters. Although serial loading is accomplished through the J and $\overline{K}$ inputs, the outputs are still routed through QA and QH. Each of the four 74199 S/Rs are eight-bit devices, and each of the bits corresponds with one decade. Therefore, each eight-bit shift register corresponds with eight decades.

A data word (in a weighted BCD format) correlates to a given decade. The word is comprised of four bits — 1, 2, 4 and 8 (i.e., 2^0, 2^1, 2^2 and 2^3 bit). Each shift register outputs one of the bits. S/R Z10 outputs the one-bit, Z9 the two-bit, Z8 the four-bit, while S/R Z7 outputs the eight bit.

For any one of the shift registers, the QA output represents the 1 ns decade, QB the 10 ns decade, QC the 100 ns decade, and so on through the 100 μs decade QF (or QH at 10 ms with the A Option, see Schematic 7065-37). But, because each shift register accommodates only eight Q outputs, and hence eight decades, an additional Quad Latch is installed to accommodate another four-bit word. Thus, the ninth decade.

An instrument is enabled for the Remote mode by moving the Remote Enable/Local switch to the Remote Enable position. With the switch in this position, the IEEE circuits are addressed and the Remote signal goes high. This signal (REM on the schematic) goes to the 74199 shift registers at pin 23, disabling the S/R parallel load inputs and thus the front-panel thumbwheel switches.

Data lines, DIO-1 through DIO-7, are divided into two functional groups. DIO1- through -4 carry numerical data whereas lines DIO-5, -6, and -7 are the "control" lines in that they are used to determine the selection of one of four data handling procedures: Memory Select, Decade Select, Numerical Data or the Execute Command. These are the commands used to select the memory register, decade space and store and retrieve information from the RAM.

NOTE

The terms Assertion and Negation are used throughout the discussion. These are discrete applications that do not follow ordinary English usage of the words. But the words are used here to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. In the present context the definitions of Assert or Assertion, Negate or Negation follow:

Assert: Indicates that a signal is active or true independent of whether that voltage is low or high.

Negate: Indicates that a signal is inactive or false.

Table 3-1 shows the various word formats for these functions in ASCII binary code, and Table 3-2 shows the actual output sequence following activation of Remote Enable.

Table 3-1. Control Lines DIO-5 through DIO-7.

Z13 (Decoder)		Function	Character Code Range			ASCII
Y5	$\overline{E}$	Execute	X0100000	to	X0101111	SP → /
Y4	$\overline{N}$	Write Data	X0110000	to	X0111001	ø → 9
Y2	$\overline{\alpha 2}$	Register Select	X1010000	to	X1011111	P → _
Y3	$\overline{\alpha 1}$	Digit Select	X1000000	to	X1001000	(α → H)

Table 3-2. IEEE Data Output Sequence.

Function	Character Code Range			Remarks
1) Address Unit	X0110000	to	X0111110	Address Cycle
2) Register Select	X1010000	to	X1011111	Data Out - 1 Cycle
3) Digit Select	X1000000	to	X1001000	Data Out - 1 Cycle
4) Write Data	X0110000	to	X0111001	Data 1 to 9 Cycle
5) Execute	X0100000	to	X0101111	Data Out - 1 Cycle
6) Unlisten	X0111111	to	---	ATN Asserted

Returning now to the circuit description: After the instrument is placed in the Remote mode, Decoder Z13 is enabled ...

1) the signals from lines DIO-5 through -7 are presented to the line decoder/ demultiplexer Z13 (74LS138), which selects one of four outputs ...
2) which are sent to inverter/buffer Z11 where they are ...
3) inverted and outputted as Select Lines Y5, Y6, Y7, Y8 ...
4) DIO-1 through -4 are presented directly to the buffer/inverter Z11 (81LS96) ...
5) and outputted onto the RAM bus.

Z13 (Decoder)	Z11 (Buffer/Inverter)	
Y5 is E, Execute	Y6	E
Y4 is N, Write Data	Y5	N
Y2 is α 2, Memory Select	Y7	α 2
Y3 is α 1, Digit Select	Y8	α 1

Line Y5 is symbolized on the schematic as "E". This line is also referred to in the text as the Update Command. The following data selection sequence constitutes the complete data entry and exit cycle to and from the RAM:

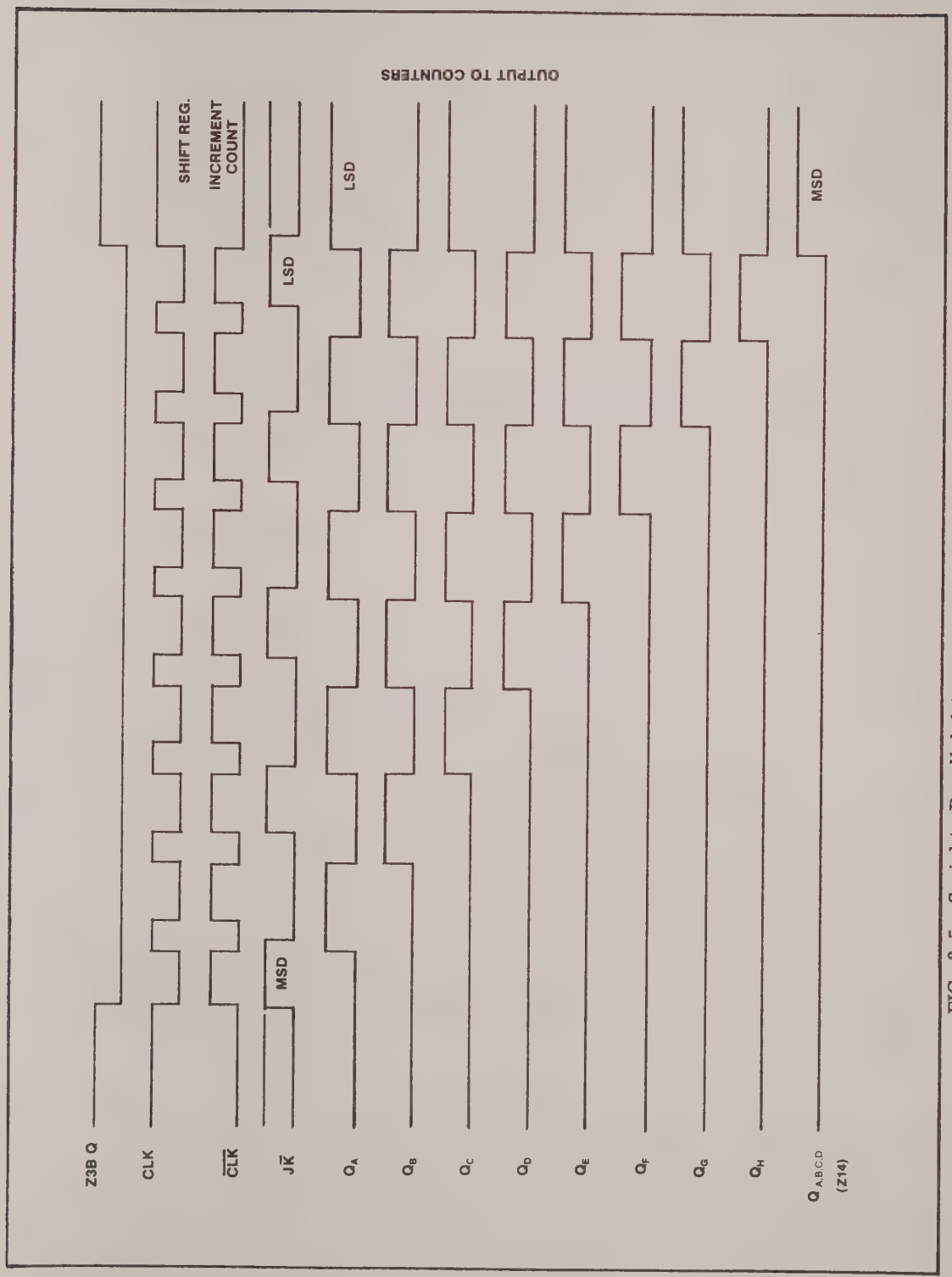


FIG. 3-5. Serial to Parallel data conversion from RAM to Shift Register with Execute (updated) command (refer to Schematic 7065-37).

1) Select the memory Register in the RAM.
2) Select the decade to be accessed in the Register.
3) Enter the data into the RAM.
4) Execute data transmission from the RAM to the shift registers.

The data selection sequence and data entry cycle are accomplished with five-key data handling functions performed by the IEEE Interface circuits. These functions are described in detail under the following headings: A. Address Cycle, B. Memory Register Select, C. Decade Select, D. Numerical Data Input, E. Execute Command, and F. Unlisten Command.

3.3.6.3 DATA HANDLING FUNCTIONS

A. Address Cycle

1) A byte is outputted onto DIO lines 1 through 8 of the format X10XXXXX
2) ATN is asserted
3) Instrument asserts NDAC
4) DAV is asserted (if valid address at Z18, pin 9, goes high)
5) Instrument negates NDAC and asserts NRFD
6) DAV is negated
7) Instrument negates NRFD and asserts NDAC
8) ATN is negated.

Lines DIO-1 through DIO-8 are outputted with a given byte format: X10XXXXX. The asserted ATN line produces a low-going pulse at the strobe ($\overline{STR}$) input of the address comparator/latch Z18. If DIO-1 through -5 are equal to the address switch settings (see Table 2-5 for valid address settings), the Z18 signal output from pin 9 goes high. This signal is then inverted by Z5E to produce a low-going signal at Z3A's Clock input, pin 9. But if, and only if, the Remote Enable switch is in the Remote Enable position, Z3A's Q-output will go high (in the Local position, Z3A's $\overline{CLR}$ input is grounded, holding Q low, which prevents remote operation). It is this output (Z3A, Q) which is the Remote (REM) line on the IEEE board that enables the control decoder (Z13), disables the Clock and parallel loading of the shift registers. The $\overline{Q}$-output of Z3A is tied to LED DS2 which illuminates when the circuits are in the Remote mode. Regardless of the output of Z3A, however, the Clock input—once the unit has been addressed with a valid address—goes low, thus illuminating DS1, and will remain in the low state until the instrument is given an Unlisten command (see Para. F).

NOTE

In this case, the instrument will have to be given an Unlisten command in order to allow a new addressing cycle to occur.

The pin 9 output of Z18 also drives NOR gate Z12A which in turn enables NAND gates Z6B and Z6D which drive lines NRFD and NDAC.

On the IEEE board, DIO lines -1 through -4 are inverted by Buffer/Inverter Z11 where they are outputted as signals D1 through D4. Simultaneously, these signals are presented to the Decade Select counter Z1's data input pins, as well as the Z15 register select latch D inputs, and the RAM (Z2) I/O inputs. Moreover, each bit is also being presented to one of the four shift registers, although the last connection is not used because data is never transferred directly from the IEEE DIO lines into the shift registers.

In the following topical descriptions, only the devices relevant to the function under discussion are mentioned. The D-1 through D-4 lines are collectively referred to as the RAM Data Bus.

B. Memory Register Select

1) A byte is outputted onto DIO lines 1 through 8 of the format X101XXXX.
2) DAV is asserted which enables decoder Z13, to assert alpha two ($\overline{\alpha 2}$).
3) DIO lines 1 through 4 and $\overline{\alpha 2}$ are inverted by Z11, thus producing signals D-1 through D-4 at the RAM Data Bus, and $\alpha 2$ at pin 1, Z16A.

When signals D-1 through D-4 are presented at the Z15 D-inputs, their numerical value determines the memory register accessed.

Alpha 2 is NANDed with $\overline{3ST}$, which produces a low at Z15's clock input. ($\overline{3ST}$ is low true, if asserted, signifying that the unit is in an Update cycle, which holds the Z16A output high, thus preventing $\alpha 2$ from passing. For now, however, assume that no Update cycle has occurred and that $\overline{3ST}$ is negated or high.) Z15's clock input is triggered on a low to high transition so at this time the Z15 outputs are unchanged.

Following these events, DAV is negated and Z13 is disabled which negates $\overline{\alpha 2}$. Alpha 2 then goes low producing a low-to-high transition at Z15's clock input. Now, Z15's Q-outputs represent the D-lines, and accordingly, the Q-outputs are presented to the four Z2 MSB address inputs to determine one of sixteen register spaces.

C. Decade Select

1) A byte is outputted onto DIO 1-8 of the format X100XXXX.
2) DAV is asserted which enables Z13 to assert $\overline{\alpha 1}$.
3) DIO 1-4 and $\overline{\alpha 1}$ are inverted by Z11 producing D1-4 on the RAM bus for the decade counter Z1, and $\alpha 1$, at Z16B, pin 5.

Alpha 1, a high-true signal, is ANDed with the $\overline{3ST}$ signal (asserted if the unit is in an Update cycle. But assume for now that the unit is not in an Update sequence). As a result, the output of NAND gate Z16B is driven low and presented to an asynchronous $\overline{LOAD}$ input of Z1, at which time the outputs of Z1 represent its inputs and are presented to the four least significant address bits of the RAM IC Z2. The DAV line is now negated by the Controller and Z13 is disabled. $\overline{Alpha\ 1}$ is driven high, $\alpha 1$ is low, thus the load signal at Z1 is removed. Z1's output count correlates to the nth-1 MSD.

D. Numerical Data Input

1) A byte is outputted onto DIO 1-8 of the format X011XXXX.
2) DAV is asserted which enables Z13 to assert $\overline{N}$.
3) DIO 1-4 and $\overline{N}$ are inverted by Z11 producing D1-4 on the RAM bus for Z2 I/O pins and N at ZC pin 5.

N is inverted at Z5C and sent to Z2's Read/Write input, as well as NAND gate Z16C. Because the signal is low-going at these points, the RAM (Z2) enters the Write mode (accepts data), and a high-going signal is produced at the output of Z16C.

The high-going signal at pin 8, Z16C, goes to the Count Up input (pin 5, Z1) which increments the count by a factor of one (1). Therefore, at the appropriate time, the data will be loaded into the RAM digit space as defined by Z1's output count.

This output from NAND gate Z16C is also presented to the inverter Z4F, the output of which is a low-going signal presented to the $\overline{\text{Chip Enable}}$ ($\overline{CE}$) input at the RAM. But at this point, resistor R8 (1.5 k) and capacitor C3 (100 pf) combine to form an RC time delay. This delay is created to prevent the RAM from being enabled during the Z1 output transitions, and thus prevents data from being loaded into incorrect digit spaces. Finally, at the conclusion of this function, the DAV line is negated, $\overline{N}$ and N are negated and the unit is ready to accept the Execute Command function.

E. Execute Command

1) A byte is outputted onto DIO lines 1 through 8 of the format X010XXXX.
2) DAV is asserted thereby enabling decoder Z13 which asserts $\overline{E}$.
3) DIO 1-4 are inverted by Z11 producing D1-4 on the RAM bus but are not used during this instruction.

Buffer/Inverter Z11 inverts $\overline{E}$ to produce E (a high-going signal) which is sent to Z1's pin 14 (CLR input) where the output is set to zero. E is also sent to the Z3B $\overline{\text{Clock}}$ ($\overline{CLK}$) input (pin 12). However, Z3B does not respond to the high-going signal since it clocks on negative-going transitions only.

The DAV line is negated by the controller and the $\overline{E}$ line returns high while E returns low. The significance of this transition is that, as E goes low, Z3B is clocked, which initiates downloading of data from the RAM, Z2, to the shift registers, Z7 through Z10.

Moreover, as Z3B is clocked, its Q-output (pin 3) goes high and the $\overline{Q}$-output goes low. The high Q-output goes to OR-gate Z12D to produce a high output, which disables Z11 and drives the $\overline{3ST}$, N and E lines low via inverters Z4C, -D and -E, respectively.

At the time the Clock is enabled, the $\overline{Q}$-output holds $\overline{DAV}$ low across the diode CR3 to prevent handshake signals NRFD and NDAC from responding to the next bus cycle, should it come along during an Execute cycle.

The low $\overline{3ST}$ signal goes to NAND-gates Z16A and B, resulting in their being disabled, which prevents inadvertent loading of the memory and digit registers. The low E prevents unintentional clearing of the Z1 digit counter. The low N is inverted which puts the RAM in the Read mode (data is outputted), enables the $\overline{Clock}$ to be presented to Z1 and enables IC Z2. Note that the Clock starts out high, then goes low and again returns high, continuing in this state for a total of nine pulses.

When the Clock is enabled, a negative transition occurs—i.e., the Clock signal is held high at pin 8, Z5D, in the disabled state until the execute command is given. Conversely, on the $\overline{Clock}$, a positive transition occurs—i.e., this signal is held low until the Clock is released and allowed to run freely. The $\overline{Clock}$ signal is presented to Z1; consequently, the count at Z1, and thus the Digit Memory Address, are then incremented.

An inverted form of the $\overline{Clock}$ enables the RAM and the RAM outputs' data stored in the address space. This data is presented to the serial inputs (J, $\overline{K}$) of the shift registers, Z7 through Z10. Each register handles one bit. Following this event, the Clock takes a positive transition and clocks the data into the shift registers.

This process continues for a total of nine counts and, on the 9-1/2 count, a look-ahead carry output is produced by the Digit Counter, Z1. The output is then subsequently presented to the asynchronous clear input of Z3B which returns the $\overline{Q}$-signal high and disables the Clock and releases DAV. At the same time, the Q-output goes low, re-enabling Z13 and negating $\overline{3ST}$, and further enabling the Memory and Digit register commands.

F. Unlisten Command

An Unlisten command will occur when the unit is addressed with the ASCII character, ? (word format X0111111). Decoder Z13 and NOR gates Z17 (A, B, C, D) are used to denote this instruction. The control bits (DIO-5, -6 and -7) select the Z13 output "N". This signal is then NORed with DIO-1 through DIO-4 and ATN. Since DIO lines -1 through -4 are low, the ATN line is asserted (low), N is selected low, and the wire-ORed outputs of Z17 (B, C, D) are high. This signal is then inverted by Z17A, and the output at pin 9, Z18, is pulled low, thus disabling the instrument. At this point, ATN is negated. Pin 9 (Z18) remains low and the unit becomes quiescent until it is either re-addressed or returned to the Local mode with the rear-panel Remote Enable/Local switch.

SECTION 4
MAINTENANCE AND CALIBRATION

4.1 INTRODUCTION

This section describes maintenance and calibration procedures for both the Model 7065 and 7075. Before attempting to troubleshoot and repair a unit, refer to the appropriate information in Section 3 for circuit detail description.

The great majority of instrument components can be replaced with standard items stocked by the local major distributors. The few exceptions include the power transformer, crystal oscillator and glass piston inductors which are available from Berkeley Nucleonics Corporation under part numbers noted in Section 5.

4.2 PREVENTIVE MAINTENANCE

The least costly and time-saving approach to reliable and accurate operation of Models 7065 and 7075 is through timely application of a preventive maintenance procedure. This includes periodic visual inspection, cleaning of controls and internal circuit boards and recalibration, if necessary. The interval for maintenance activities is largely dictated by the operating environment as well as the user's established maintenance practices and philosophy. If no established instrument maintenance schedule is currently being followed, Berkeley Nucleonics suggests following a regular schedule of timely inspection and maintenance at least once a year.

Periodically the delay generator should be inspected and cleaned of dust and grit using a jet of compressed air, vacuum or a suitable brush. In particular, be sure the fan is clear and operating properly. Discolored components and those showing obvious physical damage and deterioration should be identified and replaced. Sources which cause discoloration should be located and corrected.

4.3 CORRECTIVE MAINTENANCE

Often the cause of instrument failure or malfunction is in the power source:

- Lack of mainline power.
- A blown fuse.
- Failure of a power supply.

After turning the unit on, if there are no outputs and the power lamp doesn't light, be sure the instrument is connected to an active power source of the correct voltage. Next, check the fuse on the front panel. If these power train elements are functional, it is possible the problem is with one or more of the DC power supplies. Detailed procedures for testing and calibrating the power supplies are in Sect. 4.4.3.

4.4 CALIBRATION

4.4.1 BASIC REQUIREMENTS/TEST EQUIPMENT

NOTE

Models 7065 and 7075 should be at normal operating temperature for at least 1 hour before starting precision calibration. Adjustments to the DC power supplies, however, may be started five minutes after turn on.

The steps to calibrate the instruments must be followed in the order given. Calibration of the Models 7065 and 7075 requires attention to four principal elements whose proper adjustment is critical to accurate instrument operation. These are the:

A. Power Supplies (Para. 4.4.2).
B. VCO Voltage and Clock Frequency and C-1000 Board (Para. 4.4.3).
C. Zero Delay Coincidence (Para. 4.4.4).
D. Least Significant Decade (Para. 4.4.5).

The identification and location of adjustments for calibration, etc., are shown in Fig. 4-1 (at the end of this section).

The following test equipment, or the equivalent — with the exception of the optional Hewlett-Packard Model HP5370A — is essential for accurate calibration of the Model 7065 and 7075.

- Oscilloscope: Tektronix Model 485 (with 350 MHz bandwidth, 1 ns time division resolution).
- X 1 Oscilloscope Probe.
- Digital Multimeter/Voltmeter (DVM): Fluke Model 8022A (or other DVM with 3.5 digits).
- Frequency Counter with 1 Hz resolution.
- Digital Delay Generator: BNC Model 7050 (or other Period and Delay Generator with 100 ns resolution).
- Optional: Hewlett-Packard Model HP5370A Universal Time Interval Counter.

4.4.2 POWER SUPPLIES

Monitor all power supplies to ensure operation at specified DC-voltage levels, and to ensure acceptable AC ripple and oscillation components. In all cases, AC ripple should be less than 5 mV peak when viewed with a 20 MHz bandwidth oscilloscope. The power supplies should never exhibit any high-frequency oscillation. If any power supply voltage adjustments are necessary, they must be

made in the order listed in Table 4-1. Table 4-1 also lists the allowable tolerances for each supply, measurement test points, and the adjustment control that may affect each supply.

Table 4-1. Power Supply Adjustments and Tolerances.
NOTE: Check and adjust supplies in the sequence listed below.*

BOARD	SUPPLY	TOLERANCE	ADJUSTMENT*	WIRING POINT
7065-9	+12 (A)	12.00 V ±20 mV	R3	4
7065-9	+12 (B)	12.00 V ±1 V	No adjustment	5
7065-9	-12 (A)	-12.00 V ±0.5 V	No adjustment	7
7065-9	-12 (B)	-12.00 V ±1 V	No adjustment	9
7065-4	+5 (A)	5.00 V ±20 mV	R14	26
7065-4	+5 (B)	5.00 V ±200 mV	No adjustment	30
7065-4	-5 (A)	-5.20 V ±20 V	R18	27
7065-4	-5 (B)	-5.20 V ±20 mV	No adjustment	28
7065-4	-5 (C)	-5.20 V ±20 mV	No adjustment	29

Use the following procedure to adjust the power supplies:

1. Check +12V (A) with the DVM and adjust R3 until a reading in Table 4-1 is attained.

2. Check +12V (B), -12V (A) and (B) to be within tolerance. There are no adjustments, therefore, if out of tolerance repair is necessary.

3. Check remaining +5 and -5 volt supplies with the DVM and adjust if necessary using the appropriate potentiometers (see Table 4-1).

4. Check all nine supplies for ripple using the following method:

   a) Adjust the oscilloscope to these settings:

Time/Div.	5 ms
Display Channel 1	1 MΩ input Z
AC Coupled	
Volts/Div.	5 mV (X1)
BW Limit In	(20 MHz)
'A' Triggering	Coupling, DC Source, Line

   b) Monitor the ±12 volt supplies with the X 1 probe. Any detected ripple should be less than one division. If ripple is present or oscillation encountered, replace Z2 (LM 348). Then, repeat the previous procedure, beginning with Item 1, until the ripple reaches the prescribed level noted previously.

4.4.3 VCO VOLTAGE AND CLOCK FREQUENCY

The clock frequency and VCO voltage are initiated on the 7065-1 printed circuit board. All adjustable resistors and capacitors on the PC board not mentioned in this discussion are factory-set and their settings should not be changed.

NOTE

Before making any calibration adjustments, be sure the instrument is not triggering.

Proceed with the following steps in order.

A. TEST POINT CONNECTION:

Connect a high impedance DVM between Test Point C (TP-C) and its adjacent ground point. TP-C is located directly forward of the large metal shielding can.

B. VOLTAGE ADJUSTMENT:

The voltage at TP-C should be +1.00 volt, ±100 mV. If an adjustment is necessary, it can be made with the coil L3. The coil is located inside the shielding can. For access, use the hole in the front of the can — not the hole in the top of the can.

CAUTION

The part is fragile. Avoid any lateral pressure when making the adjustment.

C. CLOCK FREQUENCY ADJUSTMENT:

The clock frequency is checked by connecting a frequency counter (with a high-frequency probe) to TP-J, located just above Z19. The signal at this measuring point is ECL level and should be between -0.8 volt and -1.8 volts and therefore it may be difficult to trigger some counters, particularly if a 10 X probe is used. When the counter is triggering properly, check that the frequency at TP-J (pin 3, Z19) is 10.000000 MHz ±10 Hz — the clock frequency divided by 10. If the frequency exceeds the ±10 Hz tolerance, check to be sure the instrument is not being triggered. The frequency can be adjusted with coil L2 — the large glass coil located near the left-hand corner of the board. This coil is fragile and should be adjusted carefully. Most adjustments require only a fractional turn.

D. CLOCK BOARD:

First, make the following settings on the Model 7065 or 7075 front panel as applicable:

1. (Model 7075 only) Set the Trigger Mode switch to EXT TRIG but do not trigger the unit.
2. (Model 7065 and 7075) Set all the thumbwheel switches to zero (0).

Proceed with the following (if the instrument is equipped with Option B, see Para. 4.4.6, Step 2):

1. Set C12 to Min. ( )
2. Center R13 and R38.
3. Check TP-B with the DVM. Adjust the voltage to +2.50 V with R16.
4. Check TP-E with the DVM. Adjust the voltage to approximately +3.5 volts with R10.
5. Check TP-J with the frequency counter. Adjust L2 to attain 10 MHz.
6. Check TP-C with the DVM. Adjust L3 to attain +1.0 volts.
7. Trigger the Model 7065 or 7075 at 10 MHz (100 ns period). Carefully adjust R10 to attain +1.00 volts at TP-C.
8. Monitor TP-C with the DVM while varying the trigger repetition rate from 10 MHz to 500 kHz (100 ns - 2 μs period). Set the combination of Dip switches (S1) to the closed position to attain a minimum deviation from 1.0 volts at TP-C.
9. Set the Model 7050 to 10 μs in the Period mode.
10. Trigger the 7065/75 from the leading edge of the 7050's Initial Positive pulse (7065/75 slope switch set to "+").
11. Trigger the oscilloscope with the leading edge of the 7065/75's Delayed Positive pulse.
12. Set the oscilloscope to 0.2V/Div, 1 ns/Div and display the 7050's 100 MHz clock (terminated into 50 Ω) for 5 divisions peak-to-peak vertically. Center around horizontal center line and set the negative edge crossing to the vertical and horizontal center lines.
13. Sweep the 10 ns decade and adjust R38 for minimum deviation of 100 MHz clock along horizontal (deviation should be less than $\pm$ 3/10 of a division or $\pm$300 ps).
14. Sweep 100 ns and 1 μs decades and check deviation for less than $\pm$ 0.5 Div ($\pm$ 0.5 ns).

NOTE

It should be noted that, unless the Model 7050 is calibrated to its specifications, this calibration procedure may not be accurate for the longer delays. The 7065/75's oscillator and the 7050's oscillator would run at different frequencies causing an incremental error not noticeable at short delays but accumulating to a sizable error with large delays.

4.4.4 ZERO DELAY COINCIDENCE

The Initial and Delayed output pulses of the 7065 and 7075 should be adjusted so that the 50-percent amplitude points of each of the four leading edges is coincident within 100 ps when the instrument delay is set to zero (0). Certain equipment capabilities are necessary to avoid error when observing these pulses on an oscilloscope.

- The oscilloscope must have a real or effective bandwidth of at least 350 MHz (1 ns rise time) in order that the bandwidth distortion of the nominal 3 ns rise time pulse transition is reduced.
- Timing errors caused by oscilloscope channel imbalances and cable length differences must be carefully avoided (Example: See Sect. 2.4, Use of Cables...etc.)
- Proper termination is necessary to eliminate distortion caused by reflections (Proper Z = 50 Ω).

A. OUTPUT PULSE BASELINE ADJUSTMENT

With the Model 7065 or 7075 untriggered, connect a coaxial cable from the Initial Output connector to a DVM with a 200 mV scale or, an oscilloscope set to 50 mV per horizon division. Adjust R26 to attain a level as close to ground (GND) as possible. Using the same procedure, observe the Delayed and Gate outputs. Adjust the Delayed output with R9 and the Gate output with R43.

B. POSITIVE INITIAL TO POSITIVE DELAYED COINCIDENCE

On the Model 7075, first set the Initial and Delayed pulse amplitude controls fully clockwise. The Model 7065 does not have these adjustments.

1. Trigger the 7065 or 7075 at a repetition rate of approximately 100 kHz.
2. Either manually with the front-panel thumbwheel switches, or remotely through the P1 or P2 programming option, set the instrument delay to zero (0) in all decades.
3. Adjust resistor R80 on PC Board 7065-2 to move the Initial Pulse until it is coincident within ±100 ps of the Delayed Pulse at the respective 50-percent points of the leading edges.

C. POSITIVE TO NEGATIVE PULSE COINCIDENCE

Both Initial and Delayed positive and negative output pulses must be coincident at the 50-percent amplitude points of their leading edges, within a tolerance of ±100 ps. To make this adjustment, use variable capacitors C12 and C23 on PC Board 7065-3. C12 adjusts the Initial negative pulse, while C23 regulates the Delayed negative pulse. NOTE: These adjustments affect the negative pulse transitions' rise and fall times.

The specific adjustment procedures follow:

1. With C12, adjust the 50-percent point of the Initial negative pulse leading edge (the negative transition) so that it coincides with the 50-percent point of the Initial positive leading edge (the positive transition) within ±100 ps.

2. With C23, adjust the 50-percent point of the Delayed negative pulse leading edge (the negative transition) so that it coincides with the 50-percent point of the Delayed positive leading edge (the positive transition) within ±100 ps.

4.4.5 LEAST SIGNIFICANT DECADE ADJUSTMENT

Four coaxial delay lines are used to effect the 1 ns least significant decade resolution. The delay lines have nominal electrical lengths of 1 ns, 2 ns, 4 ns and 2 ns. These lines are used in a variety of combinations to produce a range of 0- to 9-ns delay in 1-ns steps. (See Table 4-2.)

The effective delay of each of the four coax lines is electrically adjusted by four variable resistors. Here are the adjustment points associated with each cable:

1 ns - R82
2 ns (A) - R87
4 ns - R88
2 ns (B) - R93

Table 4-2. Delay Line Trim Adjustments.

DELAY SETTING	ADJUSTING RESISTOR(S)			
	R82	R87	R88	R93
0 ns				
1 ns	X			
2 ns		X		
3 ns	X	X		
4 ns			X	
5 ns	X		X	
6 ns		X	X	
7 ns	X	X	X	
8 ns		X	X	X
9 ns	X	X	X	X

The accuracy of each delay, from 1 ns to 9 ns, is measured relative to a 0 ns delay. If any delay is not within tolerance, it is adjusted with the associated resistor or resistors listed in Table 4-2. However, an adjustment of any one resistor may affect other delays associated with that resistor. For example, Table 4-2 below shows that R82 and R87 are used to adjust the 3 ns setting. These same resistors are also used to adjust 1 ns and 2 ns. Thus, 1 ns and 2 ns may be affected by R82 and R87, respectively, when the 3 ns delay is re-calibrated.

If such an out of tolerance condition occurs, with respect to other affected delay settings, a compensation procedure will be necessary to adjust for the minute rise-time variations between gate outputs. Returning to the previous example: With the 3 ns setting out of tolerance, R82 and R87 are used to make the adjustment (1 ns + 2 ns = 3 ns). Thus, all other delays affected by the two resistors may also require re-adjustment. In this example, the other affected settings are 5 ns, 6 ns, 7 ns, 8 ns and 9 ns. By experimenting with subtle adjustments to the four resistors, each delay from 1 ns through 9 ns can be brought within ±100 ps of its nominal value.

4.4.6 EXTERNAL FREQUENCY REFERENCE - OPTION B

CAUTION

Calibration of the B-Option is exacting and difficult without a thorough understanding of the circuit's operation. Technicians working on the Models 7065 or 7075 should make no assumptions about, or alterations to, the B-Option calibration methods specified in this manual. No changes to these procedures should be made without first consulting Berkeley Nucleonics Corporation technical personnel.

The calibration procedure sets high- and low-limits for the reference frequency which can be locked in phase, and at the same time maintain safe operating conditions for the signal detector and varactor —Q4 and Q4, Q5 (PC Board 7065-36) respectively—safe operation being the priority.

Here is the step-by-step calibration procedure:

Note

Before starting, be sure the instrument is not triggered.

1. Measure and record the voltage levels at the varactor transistor collectors Q4, Q5 (PC Board 7065-1).

2. Check the frequency at Test Point J (TP-J, PC Board 7065-1). Adjust L1 to 10.000000 MHz. Set C12 at Max. ( ).

3. Connect an external 1 MHz signal to the 50-ohm external reference (EXT REF) terminal. Be sure that a 50-ohm termination is on the External Reference Input.

4. Place the EXT REF select switch in the 1 MHz position. The Error lamp should be off. The frequency at TP-J should be 10.000000 MHz ± proportional error of the 1 MHz EXT REF signal.

5. Measure and record the voltage at the base of Q4 (PC Board 7065-6).

6. Now, monitor the frequency at TP-J (PC Board 7065-1). Change the External Reference Input to 1.111 MHz (a 0.9 μs repetition rate) and the Error lamp should light.

7. Adjust R37 for a frequency of 10.00120 MHz at TP-J (PC Board 7065-1). At the same time, be sure the voltage at TP-D (PC Board 7065-6) does not become more negative than the voltage recorded at the base of Q4. A frequency of 10.00110 MHz is acceptable.

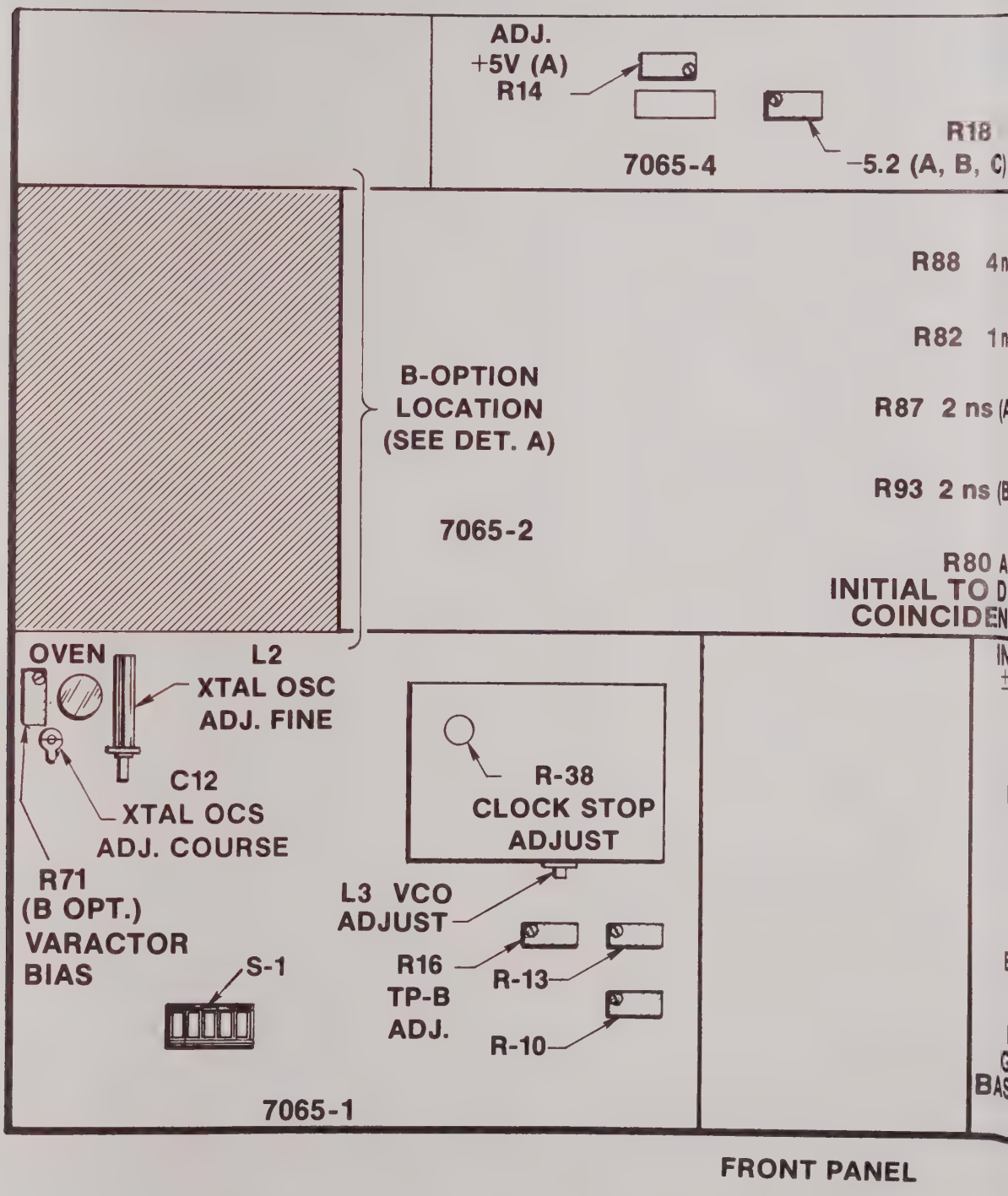
8. Change the External Reference Input to a reading of 909,090 kHz (a 1.1 μs repetition rate). The Error lamp should light.

9. Adjust R36 to a frequency of 9.999880 MHz at TP-J (PC Board 7065-1) while making sure the voltage at TP-D (PC Board 7065-6) does not become more positive than the voltage recorded at the Q4 and Q5 collectors. A frequency of 9.999890 is acceptable.

10. If the conditions stated in Steps 7 or 9 cannot be obtained, adjust the voltage at the Q4, Q5 varactor-collectors with R71*, then repeat the entire procedure beginning with Step 1.

    *Note: On the Schematic 7065-36, R71 is correct. However, on PC Board 7065-1 it is designated R130.

11. Change the EXT REF frequency to 10 MHz. The Error lamp should light. Change the EXT REF select switch to 10 MHz. The Error lamp should go off and the frequency at TP-J (PC Board 7065-1) should be 10.000000 MHz ± proportional error of the 10 MHz EXT REF signal.



Note: Dwg. not to scale. Intentionally distorted for clarity.

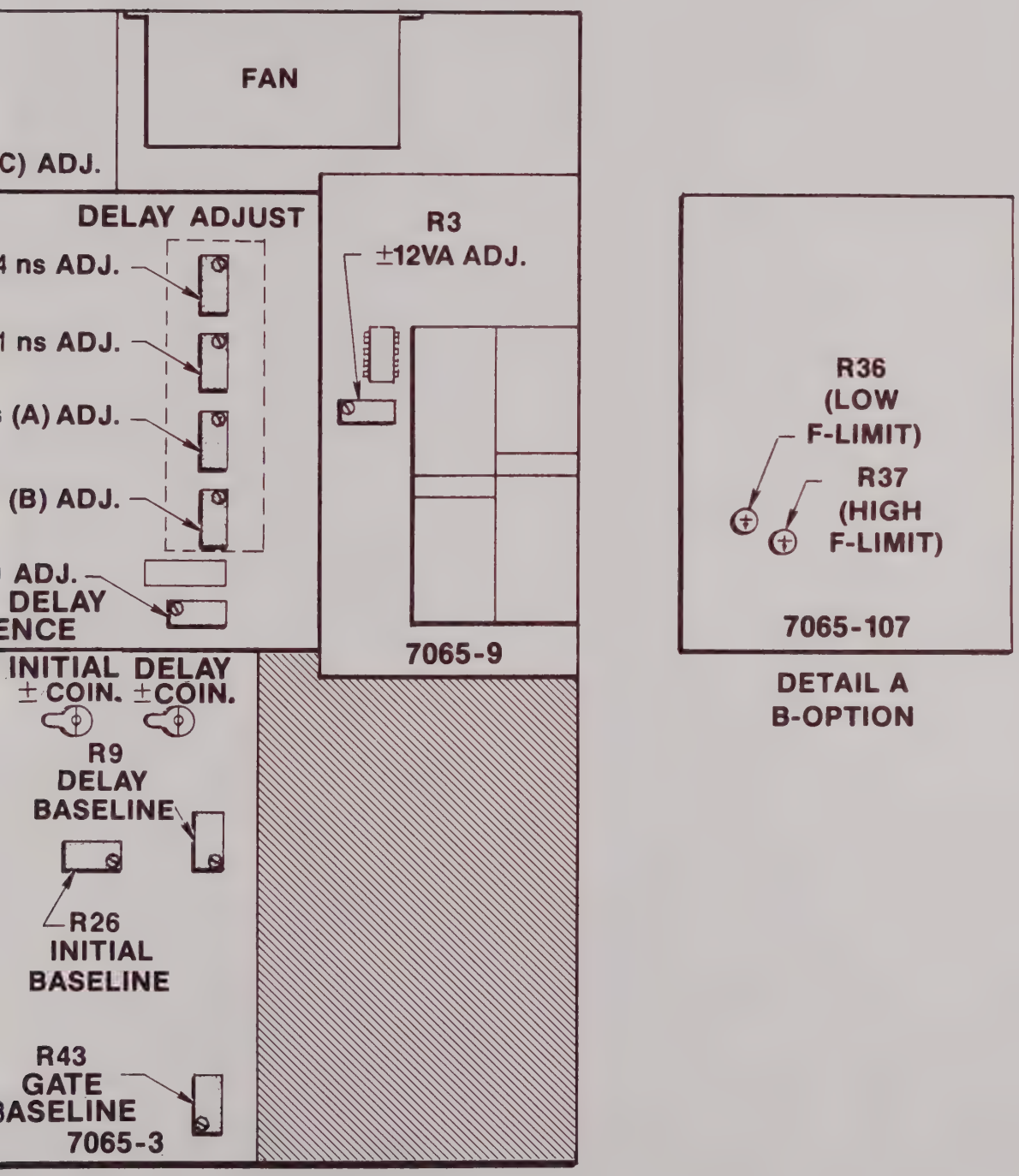


Figure 4-1. Calibration Test Points.

SECTION 5

PARTS LISTS AND SCHEMATICS

ABBREVIATIONS

cer	ceramic	μH	microhenry
comp	composition carbon	μF	microfarad
elec	electrolytic, metal case	pF	picofarad
mic	mica	pos	positions
myl	mylar	sel	selected value
k	kilohm	tan	tantalum
kV	dilovolt	V	working volts DC
M	megohm	var	variable
m	milli	W	watts
MF	metal film	ww	wirewound

---------- NOTE ----------

The last number after each part description is the BERKELEY NUCLEONICS part number for re-ordering.

PCB 7065-9 (12 V)				639-040
PCB 7065-4 (5 V)				639-104
C1	2300 μF	50 V	elec	120-015
C2	2300 μF	50 V	elec	120-015
C3	0.01 μF	16 V	cer	110-021
C4	33 μF	25 V	tan	122-015
C5	0.05 μF	25 V	cer	110-019
C6	33 μF	25 V	tan	122-015
C7	0.05 μF	25 V	cer	110-019
C8	33 μF	25 V	tan	122-015
C9	0.05 μF	25 V	cer	110-019
C10	33 μF	25 V	tan	122-015
*C11	8000 μF	15 V	elec	120-009
*C12	8000 μF	15 V	elec	120-009
*C13	33 μF	25 V	tan	122-015
*C14	0.05 μF	25 V	cer	110-019
*C15	33 μF	25 V	tan	122-015
*C16	33 μF**	25 V	tan	122-015
*C17	0.01 μF	16 V	cer	110-021
*C18	33 μF	25 V	tan	122-015
*C19	33 μF	25 V	tan	122-015
*C20	0.01 μF	16 V	cer	110-021
*C21	33 μF	25 V	tan	122-015
*C22	0.01 μF	16 V	cer	110-021
*C23	33 μF	25 V	tan	122-015

CR1		1N4005		410-001
CR2		1N4005		410-001
CR3		1N4005		410-001
CR4		1N4005		410-001
CR5		1N821	6.2 V	412-001
CR6		1N4739A	9.1 V	413-004
CR7		1N4739A	9.1 V	413-004
CR8*		1N5221, Zener	2.4 V	412-016
CR9*		1N5221, Zener	2.4 V	412-016
CR10*		1N5221, Zener	2.4 V	412-016

H1		Heat sink			527-012
H2		Heat sink, large			527-011
H3		Heat sink			527-012
H4		Heat sink			527-012
H5		Heat sink			527-012
R1	5.62 k	1/4 W	MF	1%	222-023
R2	768 Ω	1/4 W	MF	1%	222-063
R3	1 k	Pot	PCM		244-011
R4	5.62 k	1/4 W	MF	1%	222-023
R5	1 k	1/4 W	MF	1%	222-039
R6	1 k	1/4 W	MF	1%	222-039
R7	2.49 k	1/4 W	MF	1%	222-018
R8	2.49 k	1/4 W	MF	1%	222-018
R9	2.49 k	1/4 W	MF	1%	222-018
R10	2.49 k	1/4 W	MF	1%	222-018
R11*	180 Ω	1/4 W	comp	5%	213-181
R12*	4.7 k	1/4 W	comp	5%	213-472
R13*	6.19 k	1/4 W	MF	1%	222-047
R14*	1 k	Pot	PCM		244-011
R15*	4.22 k	1/4 W	MF	1%	222-045
R16*	4.7 k	1/4 W	comp	5%	213-472
R17*	4.22 k	1/4 W	MF	1%	222-045
R18*	1 k	Pot	PCM		244-011
R19*	6.19 k	1/4 W	MF	1%	222-047
R20*	4.7 k	1/4 W	comp	5%	213-472

**Options P1 & P2 only

R21*	4.7 k	1/4 W	comp	5%	213-472
R22*	1 k	1/4 W	comp	5%	213-102
R23*	1 k	1/4 W	comp	5%	213-102
R24*	1 k	1/4 W	comp	5%	213-102

Z1	7805 (w/Heat Sink)	440-023
Z2	LM348	440-068
Z3	7805 (w/Heat Sink)	440-023
Z4	7905 (w/Heat Sink)	440-047
Z5	7905 (w/Heat Sink)	440-047
Z6*	LM348	440-068
Z7*	7805 (mtd. to HS, rear)	440-023
**Z8*	7805	440-023
Z9*	7905 (mtd. to HS, rear)	440-047
Z10*	7905 (mtd. to HS, rear)	440-047
Z11*	7905 (mtd. to HS, rear)	440-047

INPUT & CLOCK SYNC ASSY. 639-042

C1	1000 pF	1 kV	cer	110-011
C2	6.8 µF	35 V	tan	122-012
C3	6.8 µF	35 V	tan	122-012
C4	33 µF	25 V	tan	122-015
C5	0.01 µF	16 V	cer	110-021
C6	6.8 µF	35 V	tan	122-012
#C7	10 pF	500 V	mic	112-016
C8	270 pF	500 V	mic	112-009
## C9	20 pF	500 V	mic	112-025
## C10	270 pF	500 V	mic	112-009
## C11	270 pF	500 V	mic	112-009
C12	7-45 pF		var	130-001
C13	22 pF	500 V	mic	112-001
C14	10 pF	1 kV	cer	110-002
C15	0.01 µF	16 V	cer	110-021
C16	0.01 µF	16 V	cer	110-021
C17	47 pF	500 V	mic	112-003
C18A	5 pF	1 kV	cer-N750	110-027
C18B	3.3 pF	500 V	cer-NPO	110-028
C19	270 pF	500 V	mic	112-009
C20	0.01 µF	16 V	cer	110-021
C21	0.01 µF	16 V	cer	110-021
C22	22 pF	500 V	mic	112-001
C23	82 pF, 500 V, mic: 7075 only			112-020
C24	100 pF, 500 V, mic: 7075 only			112-004
C25	0.01 µF	16 V	cer	110-021
C26	0.01 µF	16 V	cer	110-021
C27	0.01 µF	16 V	cer	110-021
C28	33 pF	500 V	mic	112-002
C29	33 pF	500 V	mic	112-002
C30	0.01 µF	16 V	cer	110-021
C31	0.01 µF	16 V	cer	110-021
C32	33 pF	500 V	mic	112-002
C33	33 pF	500 V	mic	112-002
C34	1000 pF	1 kV	cer	110-011
C35	0.01 µF	16 V	cer	110-021

**Options P1 & P2 only
Deleted w/B Option
Added w/B Option

C36	82 pF	500 V	mic	112-020
C37	47 pF	500 V	mic	112-003
C38	0.01 µF	16 V	cer	110-021
C39	0.01 µF	16 V	cer	110-021
C40	22 pF	500 V	mic	112-001
C41	8 pF	500 V	mic	112-015
C42	22 pF	500 V	mic	112-001
C43	33 µF	25 V	tan	122-015
C44	33 µF	25 V	tan	122-015
C45	0.01 µF	16 V	cer	110-021
C46	0.01 µF	16 V	cer	110-021
C47	0.01 µF	16 V	cer	110-021
C48	0.01 µF	16 V	cer	110-021
C49	0.01 µF	16 V	cer	110-021
C50	0.01 µF	16 V	cer	110-021
C51	0.01 µF	16 V	cer	110-021
C52	0.01 µF	16 V	cer	110-021
C53	10 pF, mic: 7075 only			112-016
C54	33 µF	25 V	tan	122-015
C55	0.01 µF	16 V	cer	110-021
C56	0.01 µF	16 V	cer	110-021
C57	0.01 µF	16 V	cer	110-021
C58	0.01 µF	16 V	cer	110-021
C59	0.01 µF	16 V	cer	110-021
C60	0.01 µF	16 V	cer	110-021
C61	0.01 µF	16 V	cer	110-021
C62	0.01 µF	16 V	cer	110-021
C63	0.01 µF	16 V	cer	110-021
C64	0.01 µF	16 V	cer	110-021
C65	0.01 µF	16 V	cer	110-021
C66	0.01 µF	16 V	cer	110-021
C67	0.01 µF	16 V	cer	110-021
C68	33 µF	25 V	tan	122-015
C69	33 µF	25 V	tan	122-015
C70	33 µF	25 V	tan	122-015
C71	0.01 µF	16 V	cer	110-021
C72	33 pF	500 V	mic	112-002

CR1	1N4152	411-001
CR2	1N4152	411-001
CR3	1N4152	411-001
CR4	1N5231B	412-009
CR5	1N5231B	412-009
CR6	1N5713	415-003
CR7	1N5713	415-003
CR8	1N5713	415-003
CR9	1N4152	411-004
CR10	1N4152	411-004
CR11	1N4152	411-004
CR12	1N4152	411-004
CR13	1N270	411-002
CR14	1N270	411-002
CR15	1N5713	415-003

DL1	28 ns Delay Line	316-016

HR1		Crystal Oven			630-003
*L1		5.6 μH			311-003
L2		0.22 μH, var			310-021
L3		0.22 μH, var			310-021
L4		0.22 μH			310-013
Q1		2N3646			430-027
Q2		2N3646			430-027
Q3		2N3646			430-027
*Q4		2 x MPS 6531			430-017
*Q5		2 x MPS 6531			430-017
Q6		2N3640			430-026
R1	470 Ω	1/4 W	comp	5%	213-471
R2	470 Ω	1/4 W	comp	5%	213-471
R3	470 Ω	1/4 W	comp	5%	213-471
R4	470 Ω	1/4 W	comp	5%	213-471
R5	470 Ω	1/4 W	comp	5%	213-471
R6	470 Ω	1/4 W	comp	5%	213-471
R7	470 Ω	1/4 W	comp	5%	213-471
R8	10 kΩ	1/4 W	comp	5%	213-103
R9	10 kΩ	1/4 W	comp	5%	213-103
R10	1 kΩ	Pot	PCM		244-011
R11	100 kΩ	1/4 W	comp	5%	213-104
R12	100 kΩ	1/4 W	comp	5%	213-104
R13	1 kΩ	Pot	PCM		244-011
R14	10 kΩ	1/4 W	comp	5%	213-103
R15	330 Ω	1/4 W	comp	5%	213-331
R16	1 kΩ	Pot	PCM		244-011
R17	130 Ω	1/4 W	comp	5%	213-131
R18	82 Ω	1/4 W	comp	5%	213-820
R19	390 Ω	1/4 W	comp	5%	213-391
R20	390 Ω	1/4 W	comp	5%	213-391
R21	240 Ω	1/4 W	comp	5%	213-241
R22	150 Ω	1/4 W	comp	5%	213-151
R23	390 Ω	1/4 W	comp	5%	213-391
R24	390 Ω	1/4 W	comp	5%	213-391
R25	390 Ω	1/4 W	comp	5%	213-391
R26	390 Ω	1/4 W	comp	5%	213-391
R27	390 Ω	1/4 W	comp	5%	213-391
R28	390 Ω	1/4 W	comp	5%	213-391
R29	390 Ω	1/4 W	comp	5%	213-391
R30	390 Ω	1/4 W	comp	5%	213-391
R31	220 Ω	1/4 W	comp	5%	213-221
R32	220 Ω	1/4 W	comp	5%	213-221
R33	100 Ω	1/4 W	comp	5%	213-101
R34	1.2 kΩ	1/4 W	comp	5%	213-122
R35	390 Ω	1/4 W	comp	5%	213-391
R36	51 Ω	1/4 W	comp	5%	213-510
R37	390 Ω	1/4 W	comp	5%	213-391
R38	500 Ω	Pot	PCM		244-010
R39	47 Ω	1/4 W	comp	5%	213-470
R40	330 Ω	1/4 W	comp	5%	213-331
R41	560 Ω	1 W	comp	5%	211-561
R42	1.2 kΩ	1/4 W	comp	5%	213-122
R43	39 Ω	1/4 W	comp	5%	213-390
R44	1.5 kΩ	1/4 W	comp	5%	213-152
R45	1.2 kΩ	1/4 W	comp	5%	213-122
R46	390 Ω	1/4 W	comp	5%	213-391
R47	390 Ω	1/4 W	comp	5%	213-391
R48	47 Ω	1/4 W	comp	5%	213-470
R49	390 Ω	1/4 W	comp	5%	213-391
R50	47 Ω	1/4 W	comp	5%	213-470
R51	470 Ω	1/4 W	comp	5%	213-471
R52	240 Ω	1/4 W	comp	5%	213-241
R53	150 Ω	1/4 W	comp	5%	213-151
R54	1 kΩ	1/4 W	comp	5%	213-102
R55	150 Ω	1/4 W	comp	5%	213-151
R56	1 kΩ	1/4 W	comp	5%	213-102
R57	1 kΩ	1/4 W	comp	5%	213-102
R58	390 Ω	1/4 W	comp	5%	213-391
**R59	10 kΩ	1/4 W	comp	5%	213-103
**R60	430 Ω	1/4 W	comp	5%	213-431
R61	47 Ω	1/4 W	comp	5%	213-470
**R62	1 kΩ	1/4 W	comp	5%	213-102
**R63	1 kΩ	1/4 W	comp	5%	213-102
**R64	150 Ω	1/4 W	comp	5%	213-151
**R65	1.5 kΩ	1/4 W	comp	5%	213-152
**R66	68 Ω	1/4 W	comp	5%	213-680
**R67	390 Ω	1/4 W	comp	5%	213-391
R68	56 Ω	1/2 W	comp	5%	212-560
R69	390 Ω	1/4 W	comp	5%	213-391
R70	91 Ω	1/4 W	comp	5%	213-910
R71	220 Ω	1/4 W	comp	5%	213-221
R72	1.2 kΩ	1/4 W	comp	5%	213-122
R73	15 kΩ	1/4 W	comp	5%	213-153
R74	3.3 kΩ	1/4 W	comp	5%	213-332
R75	120 Ω	1/4 W	comp	5%	213-121
R76	220 Ω	1/4 W	comp	5%	213-221
R77	47 Ω	1/4 W	comp	5%	213-470
R78	47 Ω	1/4 W	comp	5%	213-470
R79	390 Ω	1/4 W	comp	5%	213-391
R80	220 Ω	1/4 W	comp	5%	213-221
R81	390 Ω	1/4 W	comp	5%	213-391
R82	10 kΩ	1/4 W	comp	5%	213-103
R83	10 kΩ	1/4 W	comp	5%	213-103
R84	390 Ω	1/4 W	comp	5%	213-391
R85	1 kΩ	1/4 W	comp	5%	213-102
R86	390 Ω	1/4 W	comp	5%	213-391
R87	1 kΩ	1/4 W	comp	5%	213-102
R88	47 Ω	1/4 W	comp	5%	213-470
R89	47 Ω	1/4 W	comp	5%	213-470
R90	47 Ω	1/4 W	comp	5%	213-470
R91	47 Ω	1/4 W	comp	5%	213-470
R92	130 Ω	1/4 W	comp	5%	213-131
R93	270 Ω	1/4 W	comp	5%	213-271
R94	390 Ω	1/4 W	comp	5%	213-391
R95	390 Ω	1/4 W	comp	5%	213-391

*Added w/B Option

**Model 7075 only

R96	390 Ω	1/4 W	comp	5%	213-391
R97	47 Ω	1/4 W	comp	5%	213-470
R98	290 Ω	1/4 W	comp	5%	213-291
R99	390 Ω	1/4 W	comp	5%	213-391
R100	150 Ω	1/4 W	comp	5%	213-151
R101	240 Ω	1/4 W	comp	5%	213-241
R102	47 Ω	1/4 W	comp	5%	213-470
R103	47 Ω	1/4 W	comp	5%	213-470
R104	47 Ω	1/4 W	comp	5%	213-470
R105	2.7 kΩ	1/4 W	comp	5%	213-272
R106	1 kΩ	1/4 W	comp	5%	213-102
R107	1 kΩ	1/4 W	comp	5%	213-102
R108	1.8 kΩ	1/4 W	comp	5%	213-182
R109	1 kΩ	1/4 W	comp	5%	213-102
R110	1 kΩ	1/4 W	comp	5%	213-102
R111	10 Ω	1/4 W	comp	5%	213-100
R112	56 Ω	1/4 W	comp	5%	213-560
R113	82 Ω	1/4 W	comp	5%	213-820
R114	1.2 kΩ	1/4 W	comp	5%	213-122
R115	390 Ω	1/4 W	comp	5%	213-391
R116	390 Ω	1/4 W	comp	5%	213-391
R117	390 Ω	1/4 W	comp	5%	213-391
R118	390 Ω	1/4 W	comp	5%	213-391
R119	390 Ω	1/4 W	comp	5%	213-391
R120	200 Ω	1/4 W	comp	5%	213-201
R121	270 Ω	1/4 W	comp	5%	213-271
R122	390 Ω	1/4 W	comp	5%	213-391
R123	47 Ω	1/4 W	comp	5%	213-470
R124	390 Ω	1/4 W	comp	5%	213-391
R125	390 Ω	1/4 W	comp	5%	213-391
R126	390 Ω	1/4 W	comp	5%	213-391
R127	390 Ω	1/4 W	comp	5%	213-391
R128	240 Ω	1/4 W	comp	5%	213-241
R129	150 Ω	1/4 W	comp	5%	213-151
*R130	10 k	Pot	PCM		244-036
R131	220 Ω	1/4 W	comp	5%	213-221
R132	130 Ω	1/4 W	comp	5%	213-131
R133	82 Ω	1/4 W	comp	5%	213-820
R134	Factory Selected				
R135	2.7 Ω	1/4 W	comp	5%	213-027

S1	Dip Switch	616-001
T1	2 turns, core, (Ferrox cube)	318-003
Y1	Crystal	322-005
	Can, shield and cover	546-062

Z1	10216	440-069
Z2	10102	440-045
Z3	10102	440-045
Z4	10106	440-046
Z5	AM 685 HL	440-033
Z6	10231	440-049
Z7	AM 685 HL	440-033
Z8	10212	440-078
Z9	10102	440-045
Z10	10109	440-071
Z11	MC 1662	440-072
Z12	10125	440-041
Z13	10106	440-046
Z14	10210	440-073
Z15	10102	440-045
Z16	741	440-021
Z17	7402	440-074
Z18	10231	440-049
Z19	10138	440-077
Z20	Not Used	
Z21	10138	440-077
**Z22	10116	440-043
Z23	10212	440-078
Z24	10231	440-049
Z25	AM 685 HL	440-033

TIMING CIRCUITS, TTL & ECL 639-043

C1	0.05 μF	25 V	cer	110-019
C2	0.05 μF	25 V	cer	110-019
C3	0.05 μF	25 V	cer	110-019
C4	0.05 μF	25 V	cer	110-019
C5	0.05 μF	25 V	cer	110-019
C6	0.05 μF	25 V	cer	110-019
C7	0.05 μF	25 V	cer	110-019
C8	0.05 μF	25 V	cer	110-019
# C9	0.05 μF	25 V	cer	110-019
#C10	0.05 μF	25 V	cer	110-019
#C11	0.05 μF	25 V	cer	110-019
C12	0.05 μF	25 V	cer	110-019
C13	0.05 μF	25 V	cer	110-019
C14	33 μF	25 V	tan	122-015
C15	33 μF	25 V	tan	122-015
C16	33 μF	25 V	tan	122-015
C17	0.01 μF	16 V	cer	110-021
C18	33 μF	25 V	tan	122-015
C19	0.05 μF	25 V	cer	110-019
C20	0.01 μF	16 V	cer	110-021
C21	0.01 μF	16 V	cer	110-021
C22	0.01 μF	16 V	cer	110-021
C23	0.01 μF	16 V	cer	110-021
C24	0.01 μF	16 V	cer	110-021
C25	0.01 μF	16 V	cer	110-021
C26	0.01 μF	16 V	cer	110-021
C27	0.01 μF	16 V	cer	110-021
C28	0.01 μF	16 V	cer	110-021
C29	0.01 μF	16 V	cer	110-021
C30	0.01 μF	16 V	cer	110-021

*Added w/B Option (This part is des. R71 on 7065-36.)
**Model 7075 only

Option A only

C31	0.01 μF	16 V	cer	110-021
C32	0.01 μF	16 V	cer	110-021
C33	50 pF	1 kV	cer	110-005
C34	56 pF	500 V	mic	112-022
C35	0.01 μF	16 V	cer	110-021
C36	33 μF	25 V	tan	122-015
*C37	0.01 μF	16 V	cer	110-021
*C38	180 pF	500 V	mic	122-006
C39	Factory Selected			
C40	0.01 μF	16 V	cer	110-021
C41	0.01 μF	16 V	cer	110-021
C42	10 pF	1 kV	cer	110-023
C43	1000 pF	1 kV	cer	110-011
C44	1000 pF	1 kV	cer	110-011
C45	1000 pF	1 kV	cer	110-011
C46	1000 pF	1 kV	cer	110-011
C47	1000 pF	1 kV	cer	110-011
C48	1000 pF	1 kV	cer	110-011
C49	1000 pF	1 kV	cer	110-011
C50	1000 pF	1 kV	cer	110-011
C51	Factory Selected			
*C52	0.01 μF	16 V	cer	110-021
*C53	0.01 μF	16 V	cer	110-021
C54	10 pF	500 V	mic	112-016
C55	10 pF	500 V	mic	112-016
C56	10 pF	1 kV	cer	110-023
C57	180 pF	500 V	mic	112-006

CR1	1N5713		415-003
CR2	1N4152		411-004
CR3	1N4152		411-004
CR4	1N4152		411-004
CR5	1N4152		411-004
CR6	1N4152		411-004
CR7	Not used		

DL1	2 ns	Delay Line	TW. PR.	316-011
DL2	1 ns	BNC 7065-25		316-010
DL3	2 ns	BNC 7065-25		316-011
DL4	4 ns	BNC 7065-25		316-012
DL5	2 ns	BNC 7065-25		316-011
DL6	36 ns	Delay Line	TW. PR.	316-015

J1	Socket DIP 16-pin w/ret. clip	621-010
J2	Socket DIP 16-pin w/ret. clip	621-010
**J3	Socket DIP 16-pin w/ret. clip	621-010

L1	Inductor	0.33 μH	310-011

Q1	2N3646	430-027
*Q2	2N3640	430-026
*Q3	2N3640	430-026
Q4	2N3646	430-027
Q5	2N3646	430-027

*Model 7075 only
**Option A only

R1	5 x 22 k Network SIP					223-001
R2	5 x 22 k Network SIP					223-001
R3	5 x 22 k Network SIP					223-001
R4	5 x 22 k Network SIP					223-001
R5	5 x 22 k Network SIP					223-001
R6	5 x 22 k Network SIP					223-001
#R7	22 k	1/4 W	comp	5%		213-223
R7A/E	5 x 22 k Network SIP					223-001
#R8	22 k	1/4 W	comp	5%		213-223
R8A/E	5 x 22 k Network SIP					223-001
#R9	22 k	1/4 W	comp	5%		213-223
R9A/E	5 x 22 k Network SIP					223-001
R10	10 k	1/4 W	comp	5%		213-103
R11	1 k	1/4 W	comp	5%		213-102
R12	3.3 k	1/4 W	comp	5%		213-332
R13	82 Ω	1/4 W	comp	5%		213-820
R14	22 k	1/4 W	comp	5%		213-223
R15	10 k	1/4 W	comp	5%		213-103
R16	1 kΩ	1/4 W	comp	5%		213-102
R17	130 Ω	1/4 W	comp	5%		213-131
R18	82 Ω	1/4 W	comp	5%		213-820
R19	82 Ω	1/4 W	comp	5%		213-820
R20	130 Ω	1/4 W	comp	5%		213-131
R21	470 Ω	1/4 W	comp	5%		213-471
R22	470 Ω	1/4 W	comp	5%		213-471
R23	68 Ω	1/4 W	comp	5%		213-680
R24	470 Ω	1/4 W	comp	5%		213-471
R25	270 Ω	1/4 W	comp	5%		213-271
R26	39 Ω	1/4 W	comp	5%		213-390
R27	270 Ω	1/4 W	comp	5%		213-271
R28	82 Ω	1/4 W	comp	5%		213-820
R29	270 Ω	1/4 W	comp	5%		213-271
R30	270 Ω	1/4 W	comp	5%		213-271
R31	82 Ω	1/4 W	comp	5%		213-820
R32	470 Ω	1/4 W	comp	5%		213-471
R33	82 Ω	1/4 W	comp	5%		213-820
R34	470 Ω	1/4 W	comp	5%		213-471
R35	470 Ω	1/4 W	comp	5%		213-471
R36	249 Ω	1/4 W	MF	1%		222-011
R37	422 Ω	1/4 W	MF	1%		222-013
R38	499 Ω	1/4 W	MF	1%		222-014
R39	470 Ω	1/4 W	comp	5%		213-471
R40	68 Ω	1/4 W	comp	5%		213-680
R41	470 Ω	1/4 W	comp	5%		213-471
R42	2.7 kΩ	1/4 W	comp	5%		213-272
R43	150 Ω	1/4 W	comp	5%		213-151
R44	56 Ω	1/4 W	comp	5%		213-560
R45	1.5 kΩ	1/4 W	comp	5%		213-152
R46	470 Ω	1/4 W	comp	5%		213-471
R47	470 Ω	1/4 W	comp	5%		213-471
R48	2.7 kΩ	1/4 W	comp	5%		213-272
R49	1.5 kΩ	1/4 W	comp	5%		213-152
R50	1.3 kΩ	1/4 W	comp	5%		213-132

#Delete w/Option A

R51	270 Ω	1/4 W	comp	5%	213-271
R52	270 Ω	1/4 W	comp	5%	213-271
R53	390 Ω	1/4 W	comp	5%	213-391
*R54	270 Ω	1/4 W	comp	5%	213-271
*R55	68 Ω	1/4 W	comp	5%	213-680
*R56	100 Ω	1/4 W	comp	5%	213-101
R57	390 Ω	1/4 W	comp	5%	213-391
R58		Not used			
R59	390 Ω	1/4 W	comp	5%	213-391
R60	130 Ω	1/4 W	comp	5%	213-131
R61	82 Ω	1/4 W	comp	5%	213-820
R62	130 Ω	1/4 W	comp	5%	213-131
R63	82 Ω	1/4 W	comp	5%	213-820
R64	130 Ω	1/4 W	comp	5%	213-131
R65	82 Ω	1/4 W	comp	5%	213-820
R66	130 Ω	1/4 W	comp	5%	213-131
R67	82 Ω	1/4 W	comp	5%	213-820
R68	130 Ω	1/4 W	comp	5%	213-131
R69	82 Ω	1/4 W	comp	5%	213-820
R70	270 Ω	1/4 W	comp	5%	213-271
R71	270 Ω	1/4 W	comp	5%	213-271
R72	82 Ω	1/4 W	comp	5%	213-820
R73	130 Ω	1/4 W	comp	5%	213-131
R74	82 Ω	1/4 W	comp	5%	213-820
R75	130 Ω	1/4 W	comp	5%	213-131
R76	82 Ω	1/4 W	comp	5%	213-820
R77	130 Ω	1/4 W	comp	5%	213-131
R78	82 Ω	1/4 W	comp	5%	213-820
R79	130 Ω	1/4 W	comp	5%	213-131
R80	2 kΩ	Pot	PCM		244-035
R81	178 Ω	1/4 W	MF	1%	222-036
R82	2 kΩ	Pot	PCM		244-035
R83	178 Ω	1/4 W	MF	1%	222-036
R84	178 Ω	1/4 W	MF	1%	222-036
R85	178 Ω	1/4 W	MF	1%	222-036
R86	178 Ω	1/4 W	MF	1%	222-036
R87	2 kΩ	Pot	PCM		244-035
R88	2 kΩ	Pot	PCM		244-035
R89	178 Ω	1/4 W	MF	1%	222-036
R90	178 Ω	1/4 W	MF	1%	222-036
R91	178 Ω	1/4 W	MF	1%	222-036
R92	178 Ω	1/4 W	MF	1%	222-036
R93	2 kΩ	Pot	PCM		244-035
R94	82 Ω	1/4 W	comp	5%	213-820
R95	130 Ω	1/4 W	comp	5%	213-131
R96	270 Ω	1/4 W	comp	5%	213-271
R97	270 Ω	1/4 W	comp	5%	213-271
R98	390 Ω	1/4 W	comp	5%	213-391
R99	240 Ω	1/4 W	comp	5%	213-241
R100	390 Ω	1/4 W	comp	5%	213-391
*R101	100 Ω	1/4 W	comp	5%	213-101
*R102	68 Ω	1/4 W	comp	5%	213-680
*R103	270 Ω	1/4 W	comp	5%	213-271
R104	28 kΩ	1/4 W	MF	1%	222-024
R105	14 kΩ	1/4 W	MF	1%	222-031
R106	14 kΩ	1/4 W	MF	1%	222-031
R107	14 kΩ	1/4 W	MF	1%	222-031
R108	14 kΩ	1/4 W	MF	1%	222-031
R109	1 kΩ	1/4 W	comp	5%	213-102
R110	1 kΩ	1/4 W	comp	5%	213-102
R111	1 kΩ	1/4 W	comp	5%	213-102
R112	180 Ω	1/4 W	comp	5%	213-181
R113	220 Ω	1/4 W	comp	5%	213-221
R114	2.2 kΩ	1/4 W	comp	5%	213-222
R115	1.5 kΩ	1/4 W	comp	5%	213-152
R116	1 k	1/4 W	comp	5%	213-102
R117	150 Ω	1/4 W	comp	5%	213-151
R118	56 Ω	1/4 W	comp	5%	213-560

	Heat Sink (Thermalloy)	527-006

Z1	74190	440-036
Z2	74190	440-036
Z3	74190	440-036
Z4	74190	440-036
**Z5	74190	440-036
**Z6	74190	440-036
**Z7	74190	440-036
Z8	10124	440-070
Z9	7402	440-074
Z10	10124	440-070
Z11	74S30	440-040
Z12	10137	440-048
Z13	10125	440-041
Z14	10105	440-044
Z15	10106	440-046
Z16	10105	440-044
Z17	10515	440-079
Z18	10515	440-079
Z19	10105	440-044
Z20	10102	440-045
Z21	10515	440-079
Z22	10105	440-044
Z23	10105	440-044
Z24	LM348N	440-068

OUTPUT AMPLIFIER				639-044
C1	33 μF	25 V	tan	122-015
C2	33 μF	25 V	tan	122-015
C3	0.05 μF	25 V	cer	110-019
C4	0.05 μF	25 V	cer	110-019
C5	100 pF	500 V	mic	112-004
C6	0.05 μF	25 V	cer	110-019
C7	33 μF	25 V	tan	122-015
C8	0.05 μF	25 V	cer	110-019
C9	0.05 μF	25 V	cer	110-019
C10	33 μF	25 V	tan	122-015

*Model 7075 only
**Option A only

C11	0.05 μF	25 V	cer	110-019
C12	4.5 - 50 pF		var	130-003
C13	22 pF	500 V	mic	112-001
C14	0.05 μF	25 V	cer	110-019
C15	0.05 μF	25 V	cer	110-019
C16	100 pF	500 V	mic	112-004
C17	0.05 μF	25 V	cer	110-019
C18	33 μF	25 V	tan	122-015
C19	0.05 μF	25 V	cer	110-019
C20	0.05 μF	25 V	cer	110-019
C21	33 μF	25 V	tan	122-015
C22	0.05 μF	25 V	cer	110-019
C23	4.5 - 50 pF		var	130-003
C24	22 pF	500 V	mic	112-001
C25	0.05 μF	25 V	cer	110-019
C26	0.05 μF	25 V	cer	110-019
C27	100 pF	500 V	mic	112-004
C28	0.05 μF	25 V	cer	110-019
C29	33 μF	25 V	tan	122-015
C30	0.05 μF	25 V	cer	110-019
C31	0.05 μF	25 V	cer	110-019
C32	33 μF	25 V	tan	122-015
C33	0.05 μF	25 V	cer	110-019
C34	Not Used			
C35	0.05 μF	25 V	cer	110-019

CR1	1N4152	411-004
CR2	1N4152	411-004
CR3	1N4152	411-004
CR4	1N4152	411-004
CR5	1N4152	411-004
CR6	1N4152	411-004
CR7	1N4152	411-004
CR8	1N4152	411-004
CR9	1N4152	411-004
CR10	1N5231	412-009
CR11	1N5231	412-009
CR12	1N5231	412-009

L1	10 turns on ferrite core	318-004
L2	10 turns on ferrite core	318-004
L3	0.33 μH	310-011
L4	0.33 μH	310-011
L5	0.33 μH	310-011
L6	0.47 μH	311-005
L7	0.47 μH	311-005
L8	0.47 μH	311-005

Q1	2N3640	430-026
Q2	2N3640	430-026
Q3	2N2369	430-007
Q4	2N2369	430-007
Q5	2N2369	430-007
Q6	LT1001	430-046
Q7	2N3640	430-026
Q8	2N3640	430-026
Q9	2N2369	430-007
Q10	2N2369	430-007
Q11	2N2369	430-007
Q12	LT1001	430-046
Q13	2N3640	430-026
Q14	2N3640	430-026
Q15	2N2369	430-007
Q16	2N2369	430-007
Q17	2N2369	430-007
Q18	LT1001	430-046
*Q19	TIP34	430-029
*Q20	TIP34	430-029
Q21	TIP34	430-029

R1	150 Ω	1/4 W	comp	5%	213-151
R2	150 Ω	1/4 W	comp	5%	213-151
R3	150 Ω	1/4 W	comp	5%	213-151
R4	470 Ω	1/2 W	comp	5%	212-471
R5	33 Ω	1/4 W	comp	5%	213-330
R6	33 Ω	1/4 W	comp	5%	213-330
R7	270 Ω	1/2 W	comp	5%	212-271
R8	270 Ω	1 W	comp	5%	211-271
R9	10 kΩ	Pot	PCM		244-036
R10	1.2 kΩ	1/4 W	comp	5%	213-122
R11	220 Ω	1/2 W	comp	5%	212-221
R12	270 Ω	1/4 W	comp	5%	213-271
R13	910 Ω	1/2 W	comp	5%	212-911
R14	1.5 kΩ	1/4 W	comp	5%	213-152
R15	390 Ω	1/4 W	comp	5%	213-391
R16	51 Ω	1/4 W	comp	5%	213-510
R17	220 Ω	1/4 W	comp	5%	213-221
R18	62 Ω	1/4 W	comp	5%	213-620
R19	100 Ω	1/4 W	comp	5%	213-101
R20	180 Ω	1 W	comp	5%	211-181
R21	470 Ω	1/2 W	comp	5%	212-471
R22	33 Ω	1/4 W	comp	5%	213-330
R23	33 Ω	1/4 W	comp	5%	213-330
R24	270 Ω	1/2 W	comp	5%	212-271
R25	270 Ω	1 W	comp	5%	211-271
R26	10 kΩ	Pot	PCM		244-036
R27	1.2 kΩ	1/4 W	comp	5%	213-122
R28	220 Ω	1/2 W	comp	5%	212-221
R29	270 Ω	1/4 W	comp	5%	213-271
R30	910 Ω	1/2 W	comp	5%	212-911
R31	1.5 kΩ	1/4 W	comp	5%	213-152
R32	390 Ω	1/4 W	comp	5%	213-391
R33	51 Ω	1/4 W	comp	5%	213-510
R34	220 Ω	1/4 W	comp	5%	213-221
R35	62 Ω	1/4 W	comp	5%	213-620

*Model 7075 only

R36	100 Ω	1/4 W	comp	5%	213-101
R37	180 Ω	1 W	comp	5%	211-181
R38	470 Ω	1/2 W	comp	5%	212-471
R39	33 Ω	1/4 W	comp	5%	213-330
R40	33 Ω	1/4 W	comp	5%	213-330
R41	270 Ω	1/2 W	comp	5%	212-271
R42	270 Ω	1 W	comp	5%	211-271
R43	10 kΩ	Pot	PCM		244-036
R44	1.2 kΩ	1/4 W	comp	5%	213-122
R45	220 Ω	1/2 W	comp	5%	212-221
R46	270 Ω	1/4 W	comp	5%	213-271
R47	910 Ω	1/2 W	comp	5%	212-911
R48	1.5 kΩ	1/4 W	comp	5%	213-152
R49	390 Ω	1/4 W	comp	5%	213-391
R50	51 Ω	1/4 W	comp	5%	213-510
R51	220 Ω	1/4 W	comp	5%	213-221
R52	62 Ω	1/4 W	comp	5%	213-620
R53	100 Ω	1/4 W	comp	5%	213-101
R54	180 Ω	1 W	comp	5%	211-181
R55	1 kΩ	1/4 W	comp	5%	213-102
R56	27 Ω	1 W	comp	5%	211-270
R57	1 kΩ	1/4 W	comp	5%	213-102
R58	27 Ω	1 W	comp	5%	211-270
R59	1 kΩ	1/4 W	comp	5%	213-102
R60	27 Ω	1 W	comp	5%	211-270
*R61	180 Ω	1 W	comp	5%	211-181
*R62	180 Ω	1 W	comp	5%	211-181

THUMBWHEEL SWITCHBOARD

J1	16-pin socket w/clip		621-010
J2	16-pin socket w/clip		621-010
**J3	16-pin socket w/clip		621-010
S804	1 ns	Thumbwheel switch	610-026
S805	10 ns	Thumbwheel switch	610-026
S806	100 ns	Thumbwheel switch	610-026
S807	1 μs	Thumbwheel switch	610-026
S808	10 μs	Thumbwheel switch	610-026
S809	100 μs	Thumbwheel switch	610-026
**S810	1 ms	Thumbwheel switch	610-026
**S811	10 ms	Thumbwheel switch	610-026
**S812	100 ms	Thumbwheel switch	610-026

PANEL CONTROLS & CONNECTORS

DS801	LED	Yellow	416-004
DS802	LED	Red	416-003
J801	BNC Con.,	Trig Input	624-002
J802	BNC Con.,	Gate Out	624-002
J803	BNC Con.,	Init. Pul. Pos.Out	624-002
J804	BNC Con.,	Init.Pul.Neg.Out	624-002
J805	BNC Con.,	Del.Pul.Pos.Out	624-002
J806	BNC Con.,	Del.Pul.Neg.Out	624-002

*Model 7065 only
**Option A only

J901	50-pin Con.	Option P1 only			619-006
J901	24-pin Con.	Option P2 only			619-007
J902	BNC Con.	Option B only			624-002
R801	1 kΩ	Pot			240-008
#R802	10 k	Pot			240-015
#R803AB	500 Ω	Pot (Dual 500Ω T pad)			240-018
#R804	25 k	Pot			240-017
#R805AB	500 Ω	Pot (Dual 500Ω T pad)			240-018
#R806	25 k	Pot			240-017
#R807	51 Ω	1/2 W	comp	5%	212-510
#R808	51 Ω	1/2 W	comp	5%	212-510
#R809	51 Ω	1/2 W	comp	5%	212-510
#R810	51 Ω	1/2 W	comp	5%	212-510
S801	Toggle Switch	SPDT			611-001
S802	Pushbutton Switch				612-002
S813	Toggle Switch	PWR			611-004
S901	Slide Switch				613-002
S902	Slide Switch	Option B only			613-003
S903	Overtemp. Cutout Switch				616-002

AC Line Input

B901	Cooling Fan			631-001
#C801	10 μF	250 V	elec	120-011
#C802	1 μF	35 V	tan	122-002
#C803	0.1 μF	80 V	myl	114-029
#C804	0.1 μF	200 V	myl	114-025
#C805	0.001 μF	600 V	myl	114-001
*CR801	1N4152			411-004
#CR802	1N4152			411-004
CR901	Bridge Rectifier, PA-10			410-005
F801	Fuse	1.5 A	3 AG	634-010
#S803AB	Rotary Switch, 2-pole, 8 pos			610-024
T1	Power Transformer			320-011

OPTION B EXTERNAL REFERENCE CIRCUITS 639-046

C1	100 pF	500 V	mic	112-004
C2	0.05 μF	25 V	cer	110-019
C3	0.05 μF	25 V	cer	110-019
C4	250 pF	1 kV	cer	110-008
C5	0.01 μF	16 V	cer	110-021
C6	33 μF	25 V	tan	122-015
C7	0.05 μF	25 V	cer	110-019
C8	0.05 μF	25 V	cer	110-019
C9	0.001 μF	1 kV	cer	110-011
C10	0.05 μF	25 V	cer	110-019

#Model 7075 only

C11	0.05 μF	25 V	cer	110-019
C12	18 pF	500 V	mic	112-017
C13	250 pF	1 kV	cer	110-008
C14	0.01 μF	16 V	cer	110-021
C15	6.8 μF	35 V	tan	122-012
C16	33 μF	25 V	tan	122-015
C17	33 μF	25 V	tan	122-015
C18	33 μF	25 V	tan	122-015
C19	33 μF	25 V	tan	122-015

CR1	1N4152	411-004
CR2	1N4152	411-004
CR3	1N4152	411-004
CR4	1N4152	411-004
CR5	1N4152	411-004
CR6	1N4152	411-004
CR7	1N5231B	412-009
CR8	1N5231B	412-009
CR9	1N4152	411-004
CR10	1N4152	411-004
CR11	1N4152	411-004
CR12	1N4152	411-004

Q1	MPS 6534	430-018
Q2	MPS 6534	430-018
Q3	MPS 3646	430-027
Q4	MPS 6531	430-017

R1	150 Ω	1/4 W	comp	5%	213-151
R2	22 k	1/4 W	comp	5%	213-223
R3	22 k	1/4 W	comp	5%	213-223
R4	3.9 k	1/4 W	comp	5%	213-392
R5	6.8 k	1/4 W	comp	5%	213-682
R6	3.3 k	1/4 W	comp	5%	213-332
R7	1.5 k	1/4 W	comp	5%	213-152
R8	390 Ω	1/4 W	comp	5%	213-391
R9	220 Ω	1/4 W	comp	5%	213-221
R10	1 k	1/4 W	comp	5%	213-102
R11	82 Ω	1/4 W	comp	5%	213-820
R12	390 Ω	1/4 W	comp	5%	213-391
R13	390 Ω	1/4 W	comp	5%	213-391
R14	130 Ω	1/4 W	comp	5%	213-131
R15	82 Ω	1/4 W	comp	5%	213-820
R16	390 Ω	1/4 W	comp	5%	213-391
R17	390 Ω	1/4 W	comp	5%	213-391
R18	390 Ω	1/4 W	comp	5%	213-391
R19	390 Ω	1/4 W	comp	5%	213-391
R20	390 Ω	1/4 W	comp	5%	213-391
R21	390 Ω	1/4 W	comp	5%	213-391
R22	390 Ω	1/4 W	comp	5%	213-391
R23	3.9 k	1/4 W	comp	5%	213-392
R24	47 k	1/4 W	comp	5%	213-473
R25	10 k	1/4 W	comp	5%	213-103

*Option A only

R26	10 k	1/4 W	comp	5%	213-103
R27	4.7 k	1/4 W	comp	5%	213-472
R28	6.8 k	1/4 W	comp	5%	213-682
R29	10 k	1/4 W	comp	5%	213-103
R30	1 k	1/4 W	comp	5%	213-102
R31	10 k	1/4 W	comp	5%	213-103
R32	100 k	1/4 W	comp	5%	213-104
R33	100 Ω	1/4 W	comp	5%	213-101
R34	10 k	1/4 W	comp	5%	213-103
R35	10 k	1/4 W	comp	5%	213-103
R36	500 Ω		var		244-023
R37	500 Ω		var		244-023
R38	3.3 k	1/4 W	comp	5%	213-332
R39	56 k	1/4 W	comp	5%	213-563
R40	3.3 k	1/4 W	comp	5%	213-332
R41	82 Ω	1/2 W	comp	5%	212-820
R42	470 Ω	1/4 W	comp	5%	213-471
R43	470 Ω	1/4 W	comp	5%	213-471
R44	1 kΩ	1/4 W	comp	5%	213-102

TP	Terminal, Bifurcated	621-008

Z1	74132	440-060
Z2	74190	440-036
Z3	4044	440-076
Z4	10138	440-077
Z5	10102	440-045
Z6	10138	440-077
Z7	741	440-021

OPTION P1		639-045

C1	470 pF	500 V	mic	122-013
C2	33 μF	25 V	elec	122-015
C3	0.05 μF	25 V	cer	110-019
C4	0.05 μF	25 V	cer	110-019
C5	0.05 μF	25 V	cer	110-019
C6	0.05 μF	25 V	cer	110-019

J1	Socket DIP, 16-pin w/ret clip	621-010
J2	Socket DIP, 16-pin w/ret clip	621-010
*J3	Socket DIP, 16-pin w/ret clip	621-010
J11	Socket DIP, 16-pin w/ret clip	621-010
J12	Socket DIP, 16-pin w/ret clip	621-010
*J13	Socket DIP, 16-pin w/ret clip	621-010
J901	50-pin Conn.	619-006

R1	22 k	1/4 W	comp	5%	213-223
R2	22 k	1/4 W	comp	5%	213-223
R3	220 Ω	1/4 W	comp	5%	213-221
R4	1 k	1/4 W	comp	5%	213-102
R5	1 k	1/4 W	comp	5%	213-102

R6	22 k	1/4 W	comp	5%	213-223
R7	1 k	1/4 W	comp	5%	213-102
R8	1 k	1/4 W	comp	5%	213-102
R9	1 k	1/4 W	comp	5%	213-102
R10	1 k	1/4 W	comp	5%	213-102
R11	5 x 22 k Network SIP				223-001
R12	5 x 22 k Network SIP				223-001
R13	5 x 22 k Network SIP				223-001
R14	5 x 22 k Network SIP				223-001
R15	5 x 22 k Network SIP				223-001
R16	5 x 22 k Network SIP				223-001
*R17	5 x 22 k Network SIP				223-001
*R18	5 x 22 k Network SIP				223-001
*R19	5 x 22 k Network SIP				223-001
R20	22 k	1/4 W	comp	5%	213-223
R21	22 k	1/4 W	comp	5%	213-223
R22	5 x 22 k Network SIP				223-001
R23	5 x 22 k Network SIP				223-001
R24	5 x 22 k Network SIP				223-001
R25	22 k	1/4 W	comp	5%	213-223
R26	22 k	1/4 W	comp	5%	213-223
R27	5 x 22 k Network SIP				223-001
R28	5 x 22 k Network SIP				223-001
R29	5 x 22 k Network SIP				223-001
*R30	5 x 22 k Network SIP				223-001
*R31	5 x 22 k Network SIP				223-001
*R32	22 k	1/4 W	comp	5%	213-223
*R33	22 k	1/4 W	comp	5%	213-223

Z1	7475	440-016
Z2	74157	440-075
Z3	7475	440-016
Z4	74157	440-075
Z5	7475	440-016
Z6	74157	440-075
Z7	7475	440-016
Z8	74157	440-075
Z9	7475	440-016
Z10	74157	440-075
Z11	7475	440-016
Z12	74157	440-075
*Z13	7475	440-016
*Z14	74157	440-075
*Z15	7475	440-016
*Z16	74157	440-075
*Z17	7475	440-016
*Z18	74157	440-075
Z19	7400	440-027
Z20	7416	440-063

*Option A only

OPTION P2

C1	330 pF	500 V	mic	112-010
C2	270 pF	500 V	mic	112-009
C3	100 pF	500 V	mic	112-004
C4	100 pF	500 V	mic	112-004
C5	6.8 μF	35 V	tan	122-012
C6	0.05 μF	16 V	cer	110-019
C7	0.05 μF	16 V	cer	110-019
C8	6.8 μF	35 V	tan	122-012
C9	0.05 μF	16 V	cer	110-019
C10	0.05 μF	16 V	cer	110-019
C11	33 μF	25 V	tan	122-015
C12	0.05 μF	16 V	cer	110-019
C13	0.05 μF	16 V	cer	110-019
C14	33 μF	25 V	tan	122-015

CR1	1N270	411-002
CR2	1N270	411-002
CR3	1N270	411-002
CR4	1N270	411-002

DS1	Socket, 16-pin DIP 45° angle	621-012

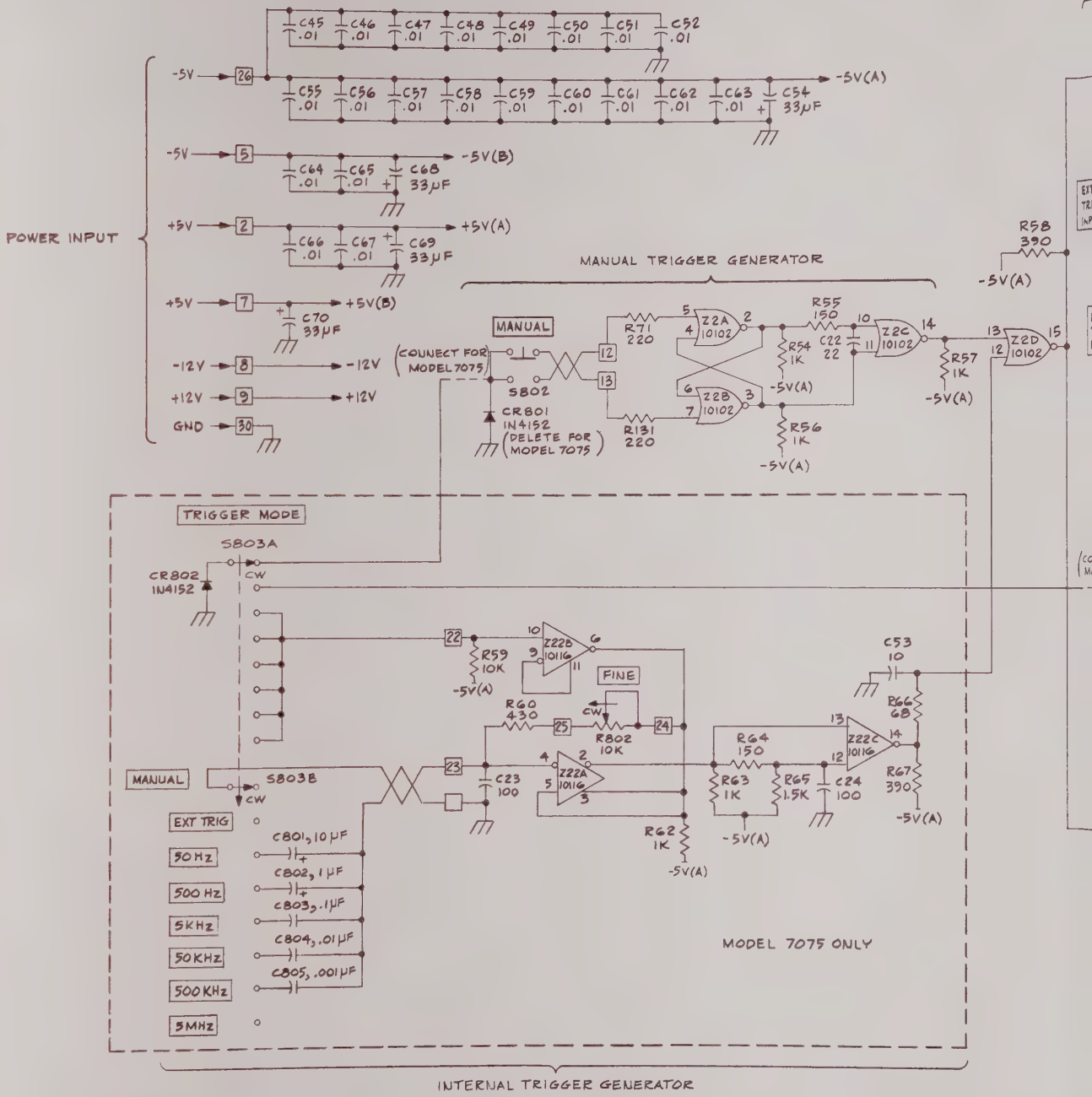
J1	Socket, 16-pin DIP w/ret clip	621-010
J2	Socket, 16-pin DIP w/ret clip	621-010
*J3	Socket, 16-pin DIP w/ret clip	621-010
J11	Socket, 16-pin DIP w/ret clip	621-010
J12	Socket, 16-pin DIP w/ret clip	621-010
*J13	Socket, 16-pin DIP w/ret clip	621-010
J901	24-pin Conn.	619-007

Q1	2N3646	430-027

R1	3 k & 6.2 k Network 16-pin DIP				223-004
R2	2.7 k	1/4 W	comp	5%	213-272
R3	1.5 k	1/4 W	comp	5%	213-152
R4	2.7 Ω	1/4 W	comp	5%	213-027
R5	560 Ω	1/4 W	comp	5%	213-561
R6	1.5 k	1/4 W	comp	5%	213-152
R7	1.5 k	1/4 W	comp	5%	213-152
R8	1.5 k	1/4 W	comp	5%	213-152
R9	1.5 k	1/4 W	comp	5%	213-152
R10	560 Ω	1/4 W	comp	5%	213-561
R11	560 Ω	1/4 W	comp	5%	213-561
R12	22 k	1/4 W	comp	5%	213-223
R13	2.7 Ω	1/4 W	comp	5%	213-027
R14	1.5 k	1/4 W	comp	5%	213-152
R15	1.5 k	1/4 W	comp	5%	213-152
R16	22 k	1/4 W	comp	5%	213-223
R17	1.5 k	1/4 W	comp	5%	213-152
R18	1 k	1/4 W	comp	5%	213-102
R19	1.5 k	1/4 W	comp	5%	213-152
R20	5 x 22 k Network SIP				223-001

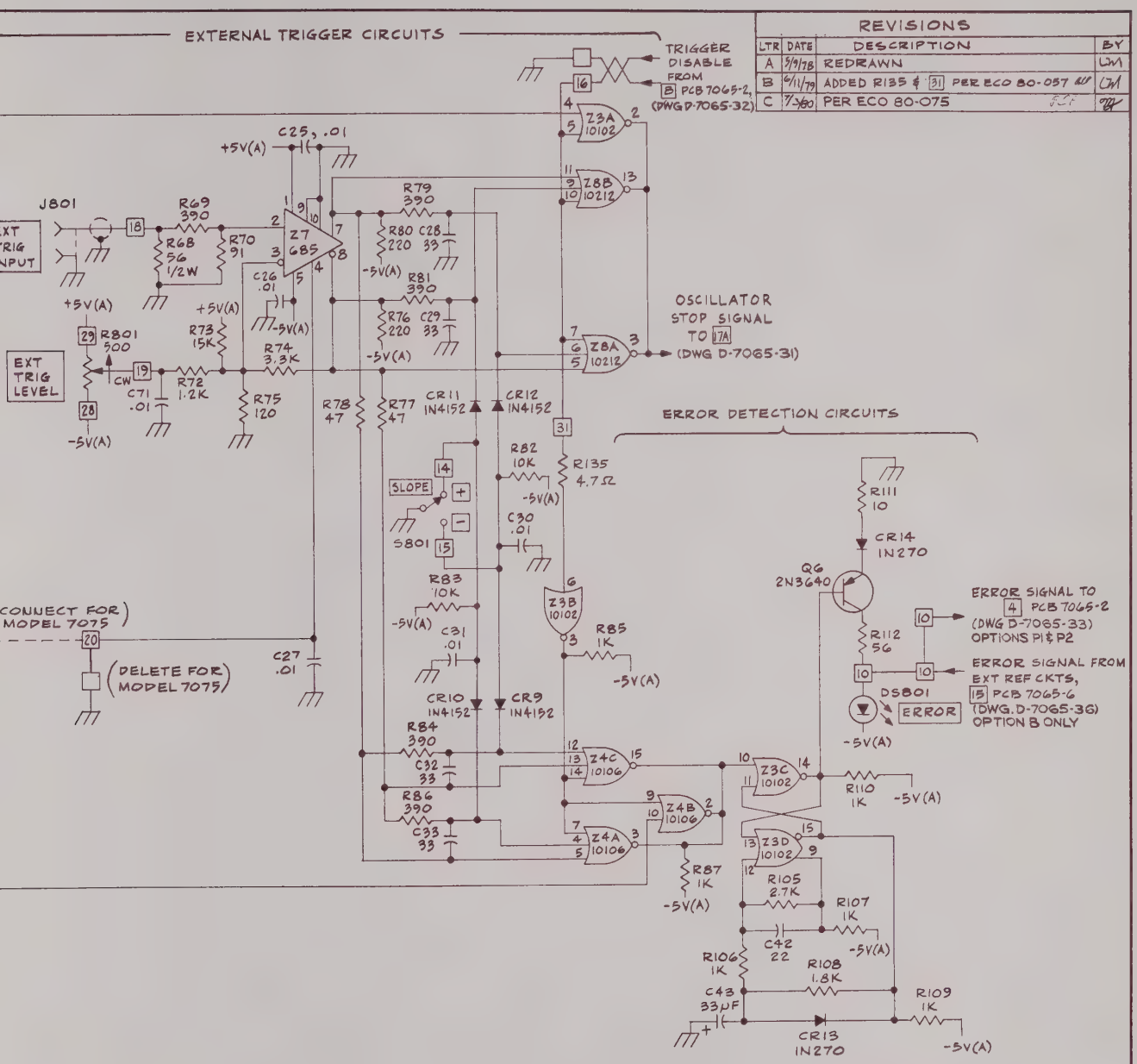
R21	3.3 k	1/4 W	comp	5%	213-332
R22	6.8 k	1/4 W	comp	5%	213-682
R23	22 k	1/4 W	comp	5%	213-223
R24	10 k	1/4 W	comp	5%	213-103
R25	1.5 k	1/4 W	comp	5%	213-152
R26	5 x 22 k Network SIP				223-001
R27	5 x 22 k Network SIP				223-001
R28	5 x 22 k Network SIP				223-001
R29	5 x 22 k Network SIP				223-001
R30	5 x 22 k Network SIP				223-001
R31	5 x 22 k Network SIP				223-001
R32	5 x 22 k Network SIP				223-001
R33	5 x 22 k Network SIP				223-001
S1	DIP Switch, 8				616-001
S2	Toggle Switch				611-007

Z1	74S192	440-089
Z2	2112 RAM	440-091
Z3	74LS107	440-086
Z4	74LS05	440-081
Z5	74LS14	440-082
Z6	7438	440-085
Z7	74199	440-090
Z8	74199	440-090
Z9	74199	440-090
Z10	74199	440-090
Z11	81LS96	440-093
Z12	74LS32	440-083
Z13	74LS138	440-087
Z14	74LS298	440-107
Z15	74LS175	440-088
Z16	74LS03	440-080
Z17	74LS33	440-084
Z18	8136	440-092



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE 1/4W, 5%
   ALL CAPACITORS < 1.0 ARE IN µF AND > 1.0 ARE IN pF.
2. IC POWER AND GROUND CONNECTIONS NOT ON SCHEMATIC ARE LISTED IN TABLE I.
3. ⊙ DENOTES PCB TEST POINT.
4. □ DENOTES PCB WIRING CONNECTIONS
5. ▭ DENOTES FRONT PANEL NOMENCLATURE.
6. ⋈ TWISTED PAIR TRANSMISSION LINES
7. ALL COMPONENTS CARRYING "800" SERIES NO'S ARE LOCATED ON FRONT PANEL AND ARE REF. ONLY.



REVISIONS			
LTR	DATE	DESCRIPTION	BY
A	5/9/78	REDRAWN	LM
B	6/11/79	ADDED R135 & 31 PER ECO 80-057	LM
C	7/3/80	PER ECO 80-075	

REF : PCB 7065-1

TPA	TPF	
S1	S1	
R1	R134	R61, R127
Q1	Q6	
L1	L4	
J801	J801	
HR1	HR1	
DS801	DS801	
DL1	DL1	
CR1	CR15	
C1	C72	C44,
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

TABLE 1

IC POWER & GROUND CONNECTIONS			
IC NO.	GND PIN	PWR PIN	PWR SOURCE
Z8	1, 15, 16	8	-5V (A)
Z2-Z4 Z22	1, 16	8	-5V (A)

Z1	Z25	Z20
Y1	Y1	
T1	T1	
FIRST	LAST	OMITTED

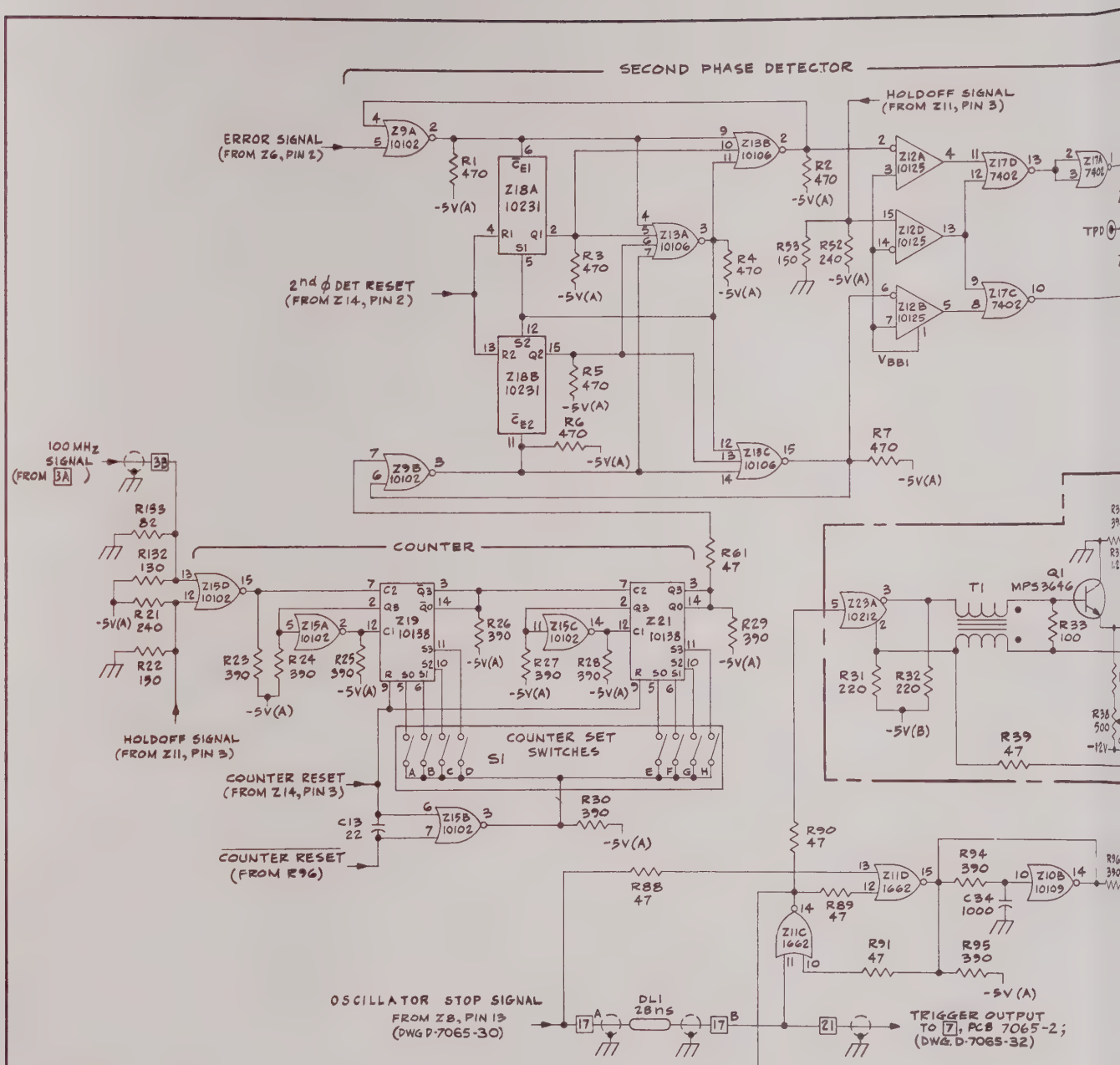
REFERENCE DESIGNATIONS (CONT.)

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: NONE | APPROVED BY: GWR 3-25-79 | DRAWN BY: LM
DATE: 5/9/78 | REVISED

DIGITAL DELAY GENERATORS, MODEL 7065/75

INPUT CIRCUITS | D | DRAWING NUMBER 7065-30C

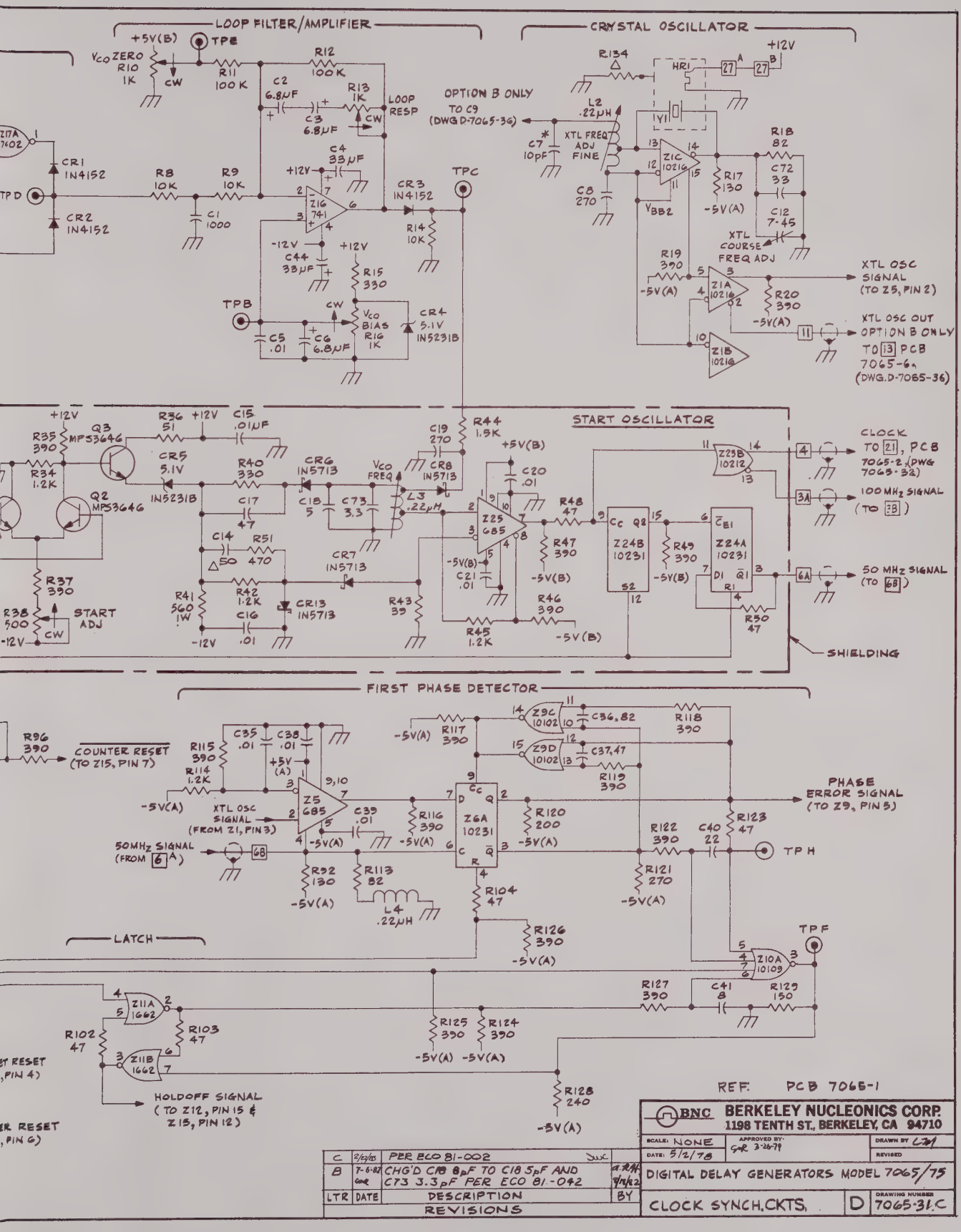


NOTES:
UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE ¼ W, 5 %.
2. ALL CAPACITORS < 1.0 ARE IN μf AND > 1.0 ARE IN pf.
3. IC POWER AND GROUND CONNECTIONS NOT ON SCHEMATIC ARE LISTED IN TABLE I.
4. * DELETE FOR OPTION B.
5. □ DENOTES PCB WIRING CONNECTIONS.
6. Ⓣ DENOTES PCB TEST POINT
7. REFERENCE DESIGNATIONS ARE LOCATED ON DWG 7065-30.
8. △ DENOTES FACTORY SELECTED COMPONENT.

TABLE I

IC POWER & GROUND CONNECTIONS			
IC NO.	GND. PIN	PWR PIN	PWR SOURCE
Z 17	7	14	+5V (A)
Z 12	16	8 (9)	-5V(A), [-5V(A)]
Z 14	1, 15, 16	8	-5V (A)
Z1, Z6, Z9-Z11, Z13, Z15, Z18, Z19, Z21	1, 16	8	-5V (A)
Z 24	1, 16	8	-5V (B)
Z 23	1, 15, 16	8	-5V (B)



LTR	DATE	DESCRIPTION	BY
C	2/23/78	PER ECO 81-002	JWC
B	7-6-82	CHG'D C18 8pF TO C18 5pF AND C73 3.3pF PER ECO 81-042	a.R.H. 7/16/82

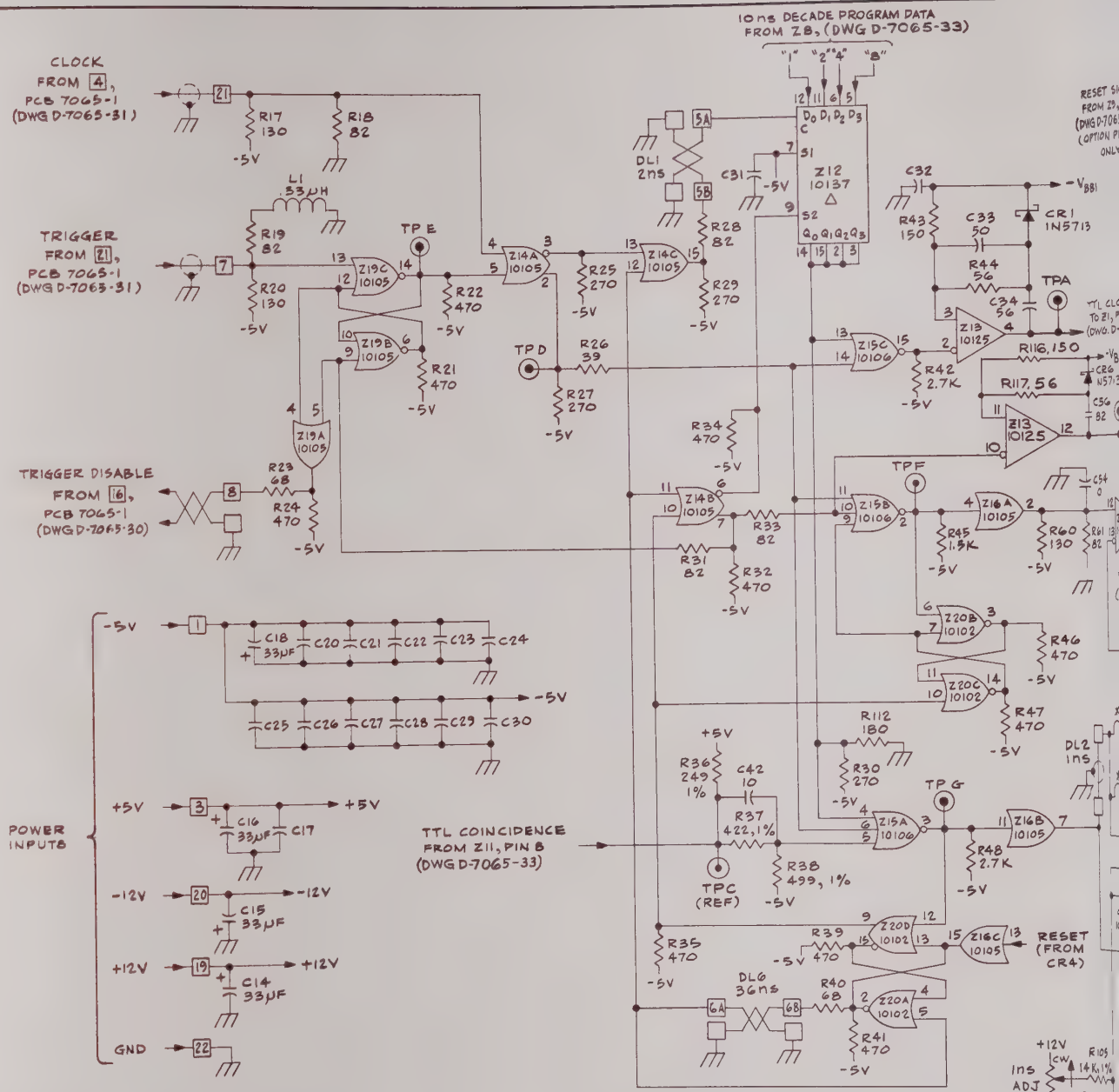
REVISIONS

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: NONE	APPROVED BY: GLR 3-26-79	DRAWN BY: CJM
DATE: 5/2/78		REVISED

DIGITAL DELAY GENERATORS MODEL 7065/75

CLOCK SYNCH.CKTS. | D | DRAWING NUMBER 7065-31.C



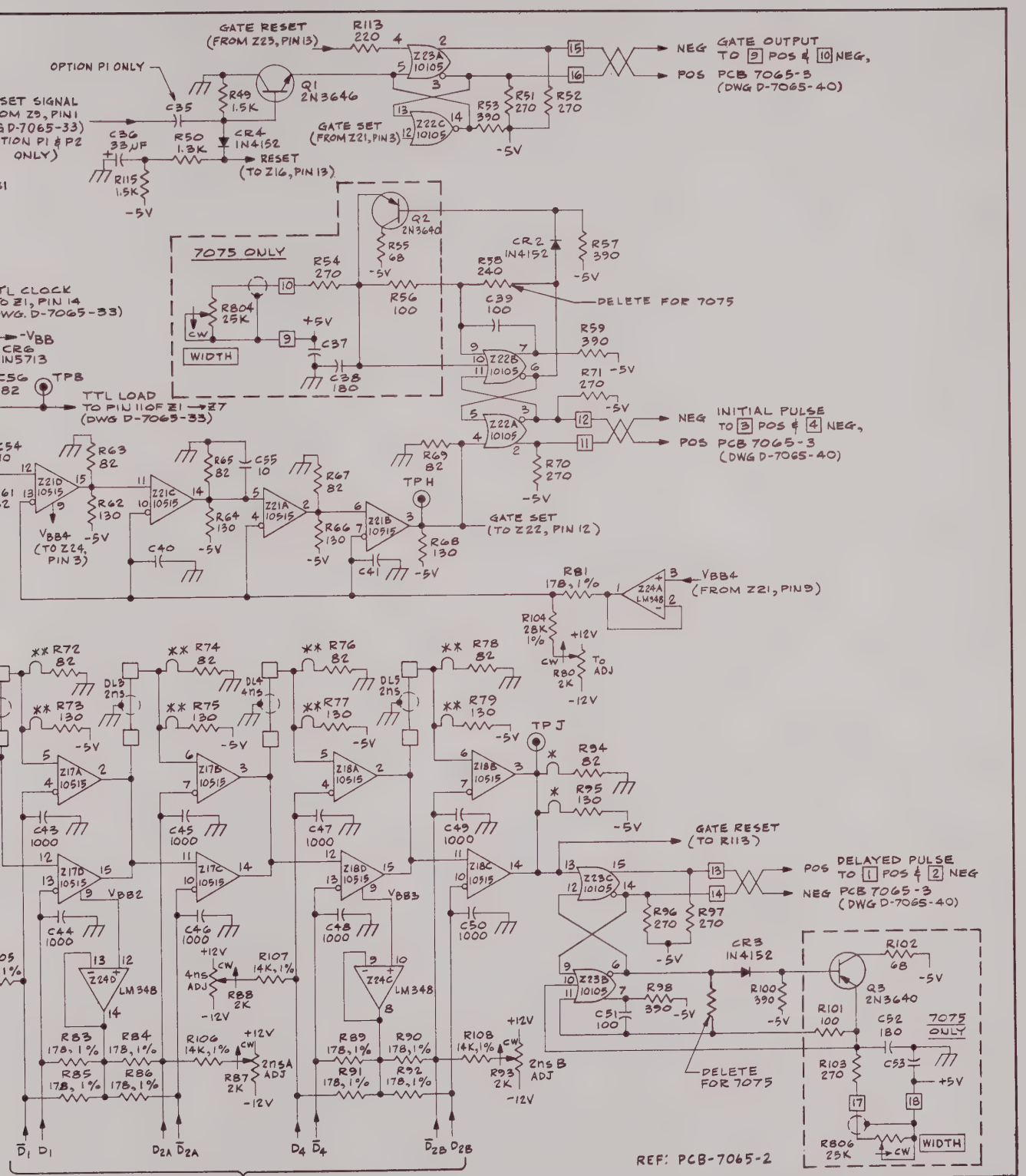
NOTES:

UNLESS OTHERWISE SPECIFIED:

1. IC PWR & GND CONNECTIONS ARE SHOWN IN TABLE I.
2. ALL RESISTORS ARE 1/4 W, 5%.
3. ALL CAPACITORS ARE .01μF ON DWG 7065-32. ALL CAPACITORS ARE .05μF ON DWG 7065-33.
4. ALL CAPACITORS < 1.0 ARE IN μF, > 1.0 ARE IN pF.
5. XX INDUCTANCE FORMED BY RESISTOR LEADS.
6. □ DENOTES PC BOARD TERMINALS.
7. ▭ DENOTES FRONT PANEL LETTERING.
8. ⋈ DENOTES TWISTED PAIR TRANSMISSION LINE.
9. ⊙ DENOTES TEST POINT.
10. REFERENCE DESIGNATIONS ARE ON DWG NO 7065-33
11. △ DENOTES HEAT SINK ON COMPONENT.

TABLE I

IC POWER & GROUND CONNECTIONS			
IC NO.	GND PIN(S)	PWR PIN(S)	PWR SOURCE(S)
Z13	16	8 (9)	-5V (+5V)
Z 24	–	11 (4)	-12V (+12V)
Z12, Z14-23	1, 16	8	-5V
Z1-7, Z9	7	14	+5V
Z8, Z10	16	8 (9)	-5V (+5V)



LTR	DATE	DESCRIPTION	BY	CHKD
A	9-5-80	PER ECO 80-083	RP	

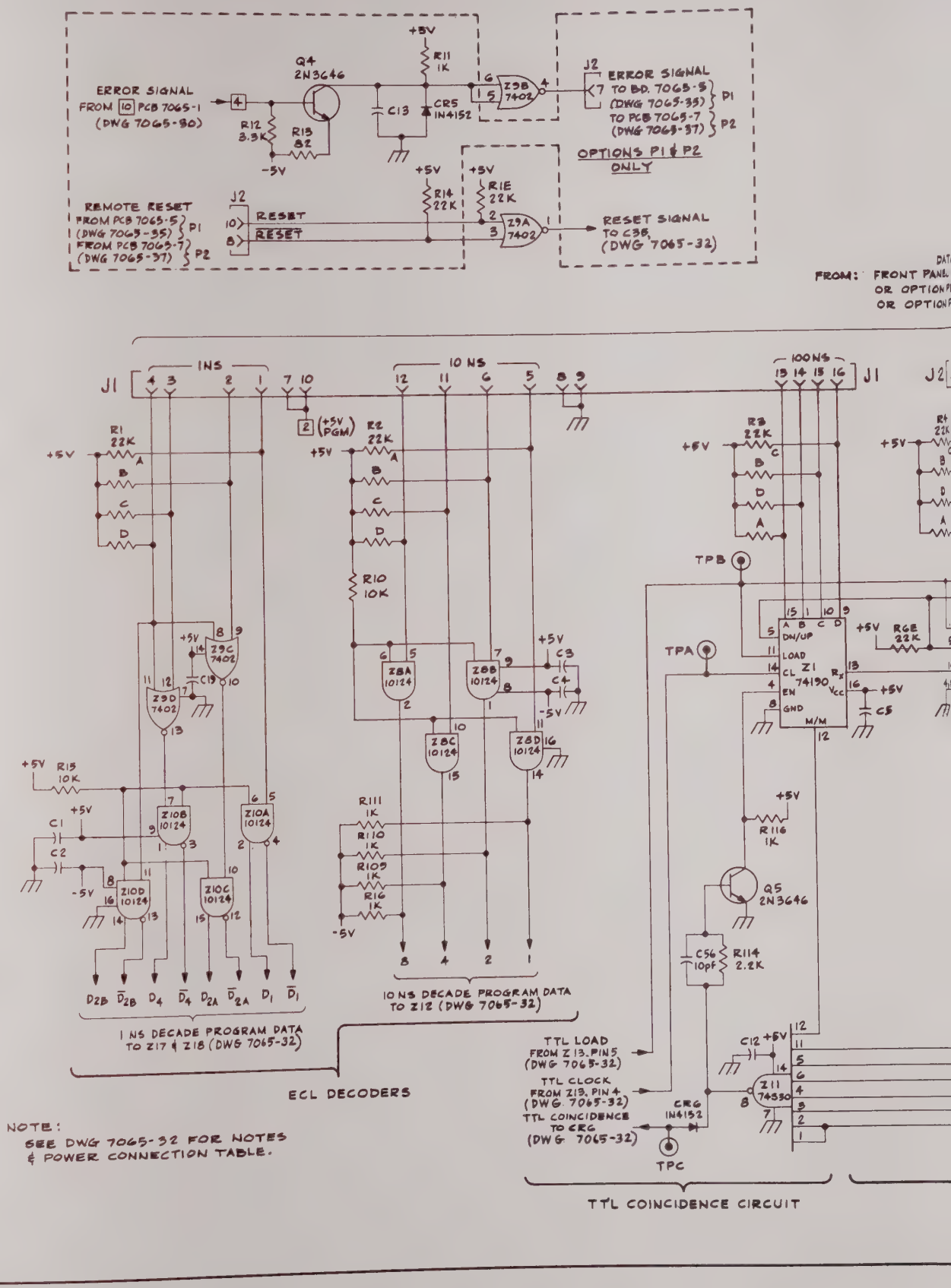
REVISIONS

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: ∞	APPROVED BY:	DRAWN BY CM
DATE: 3-30-79	K. LP	REVISED

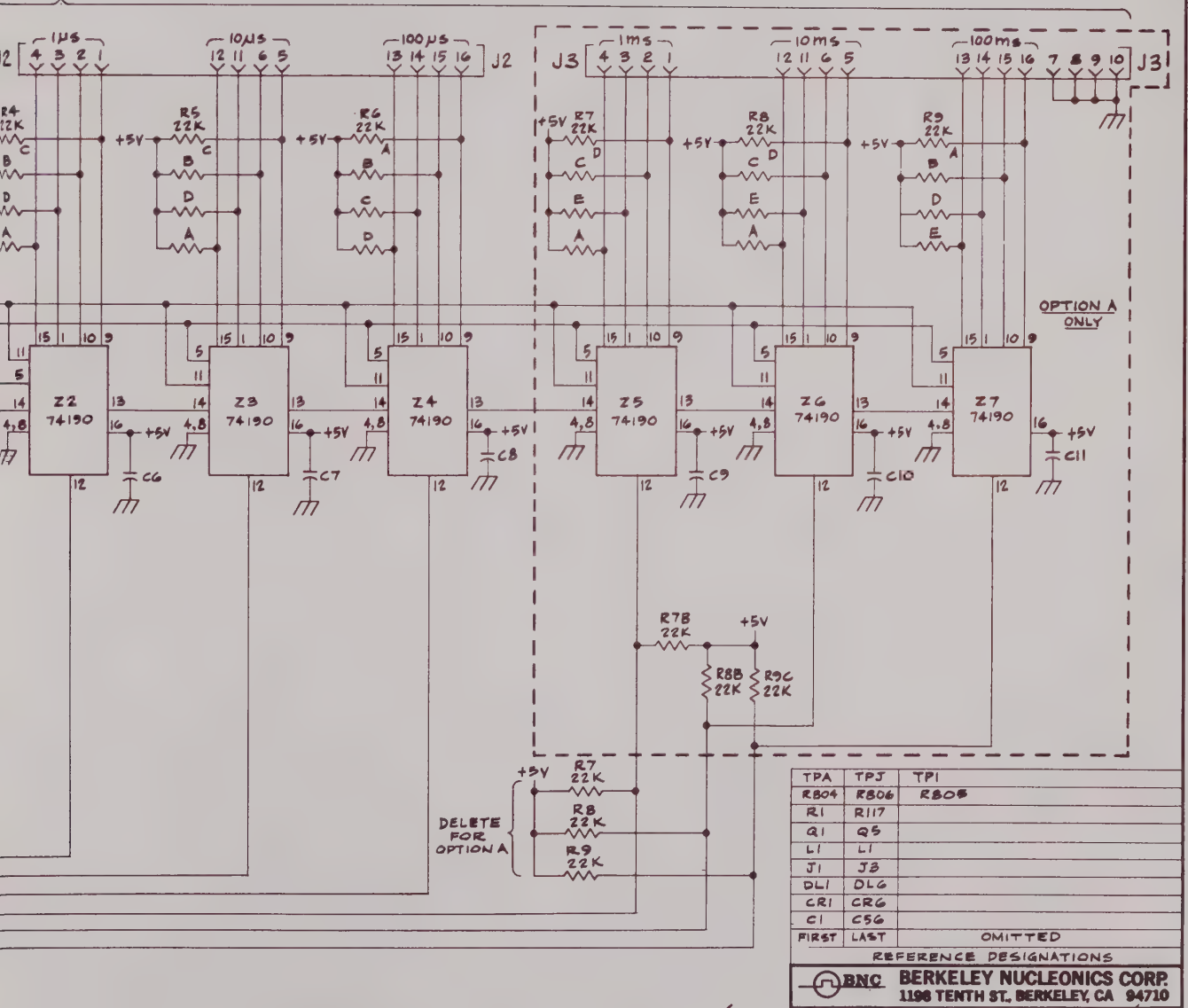
DIGITAL DELAY GENERATOR MOD. 7065/75

TIMING CIRCUITS (ECL) | D | DRAWING NUMBER 7065-32 A


ERROR SIGNAL FROM 10 PCB 7065-1 (DWG 7065-30)
Q4 2N3646
R11 1K
+5V
R12 3.3K
R13 82
-5V
C13
CR5 IN4152
Z9B 7402
J2
ERROR SIGNAL TO BD. 7065-5 (DWG 7065-35) P1
TO PCB 7065-7 (DWG 7065-37) P2
OPTIONS P1 & P2 ONLY
REMOTE RESET FROM PCB 7065-5 (DWG 7065-35) P1
FROM PCB 7065-7 (DWG 7065-37) P2
RESET
RESET
R14 22K
R1E 22K
Z9A 7402
RESET SIGNAL TO C38, (DWG 7065-32)
FROM: FRONT PANEL OR OPTION P1 OR OPTION P2
J1
1NS
10 NS
100NS
R1 22K
R2 22K
R3 22K
R10 10K
R15 10K
R111 1K
R110 1K
R109 1K
R16 1K
R116 1K
R114 2.2K
C56 10pF
C1
C2
C3
C4
C5
C12
C19
Z8A 10124
Z8B 10124
Z8C 10124
Z8D 10124
Z10A 10124
Z10B 10124
Z10C 10124
Z10D 10124
Z9C 7402
Z9D 7402
Z1 74190
Z11 74S30
Q5 2N3646
CR6 IN4152
TPA
TPB
TPC
RGE 22K
D2B D2B D4 D4 D2A D2A D1 D1
1 NS DECADE PROGRAM DATA TO Z17 & Z18 (DWG 7065-32)
10 NS DECADE PROGRAM DATA TO Z12 (DWG 7065-32)
ECL DECODERS
TTL LOAD FROM Z13, PIN 5 (DWG 7065-32)
TTL CLOCK FROM Z13, PIN 4 (DWG 7065-32)
TTL COINCIDENCE TO CR6 (DWG 7065-32)
TTL COINCIDENCE CIRCUIT
NOTE:
SEE DWG 7065-32 FOR NOTES & POWER CONNECTION TABLE.

REVISIONS			
LTR	DATE	DESCRIPTION	BY
A	9/22/77	UPDATE	SR
B	4/19/78	REDRAWN	LM

DATA INPUT
NEL THUMBWHEEL SWITCHES (DWG 7065-38)
ON P1 (DWG 7065-35)
ION P2 (DWG 7065-37)



TPA	TPJ	TPI
RB04	RB06	RB08
R1	R117	
Q1	Q5	
L1	L1	
J1	J8	
DL1	DL6	
CR1	CR6	
C1	C56	
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

TTL COUNTERS

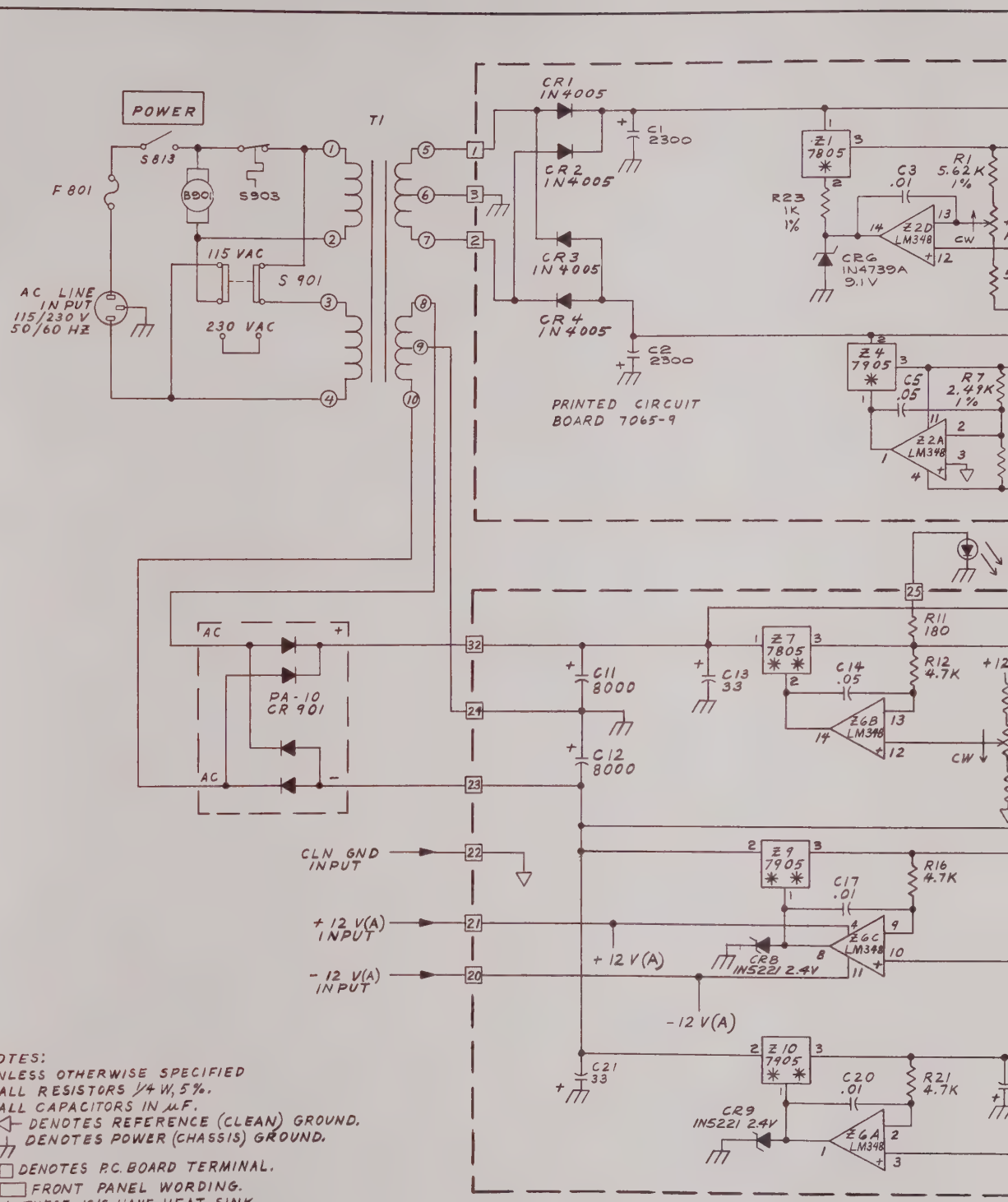
REF: PCB 7065-2

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

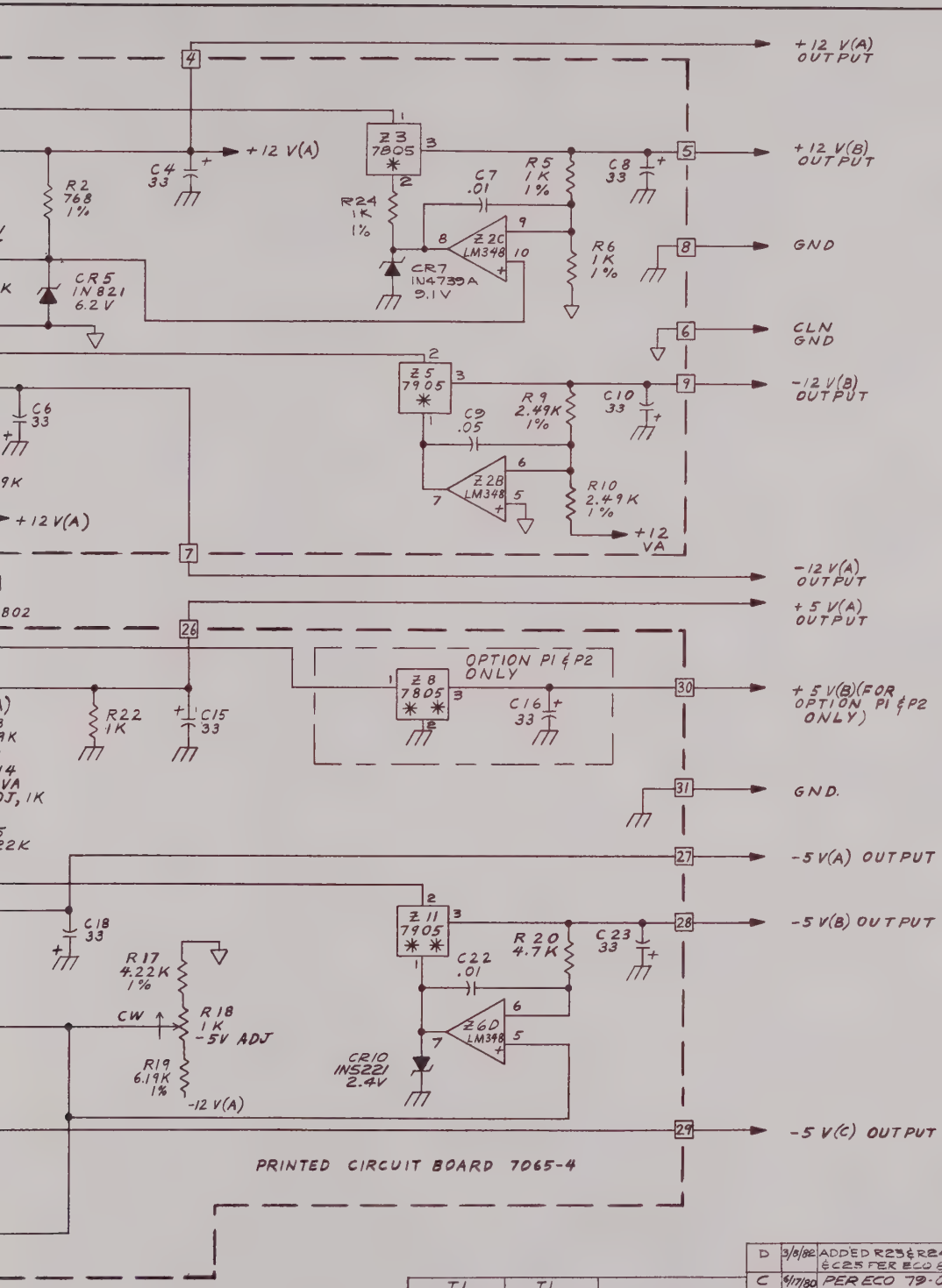
SCALE: ~	APPROVED BY: GdR	DRAWN BY: EM
DATE: 4/20/78		REVISED

DIGITAL DELAY GENERATORS, MODEL 7065/75

TIMING CIRCUITS, TTL	D	DRAWING NUMBER 7065-33B



NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS 1/4 W, 5%.
2. ALL CAPACITORS IN μF.
3. ◁ DENOTES REFERENCE (CLEAN) GROUND.
4. ⏚ DENOTES POWER (CHASSIS) GROUND.
5. □ DENOTES P.C. BOARD TERMINAL.
6. ▭ FRONT PANEL WORDING.
7. ✳ THESE IC'S HAVE HEAT SINK.
8. ✳✳ THESE IC'S MOUNTED TO HEAT SINK, REAR PANEL.



T1	T1	
B901	B901	
S813, S901	S813, S903	S902
F801	F801	
DS 802	DS 802	
Z1	Z6	
CR1, CR901	CR10, CR901	
C1	C23	C24, C25
R1	R24	
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

LTR	DATE	DESCRIPTION	BY
D	3/8/82	ADDED R23 & R24; OMITTED C24 & C25 PER ECO 82-010, 82-031	
C	9/17/80	PER ECO 79-034	RAP
B	9/11/80	R15 WAS 22K, NOW: 4.22K	RAP

REVISION BLOCK

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: —	APPROVED BY: GWR 3-8-79	DRAWN BY G.J.
DATE: 10-30-78		REVISED

DIGITAL DELAY GENERATOR MODELS 7065-7075

POWER SUPPLY SCHEM. D DRAWING NUMBER 7065-34D

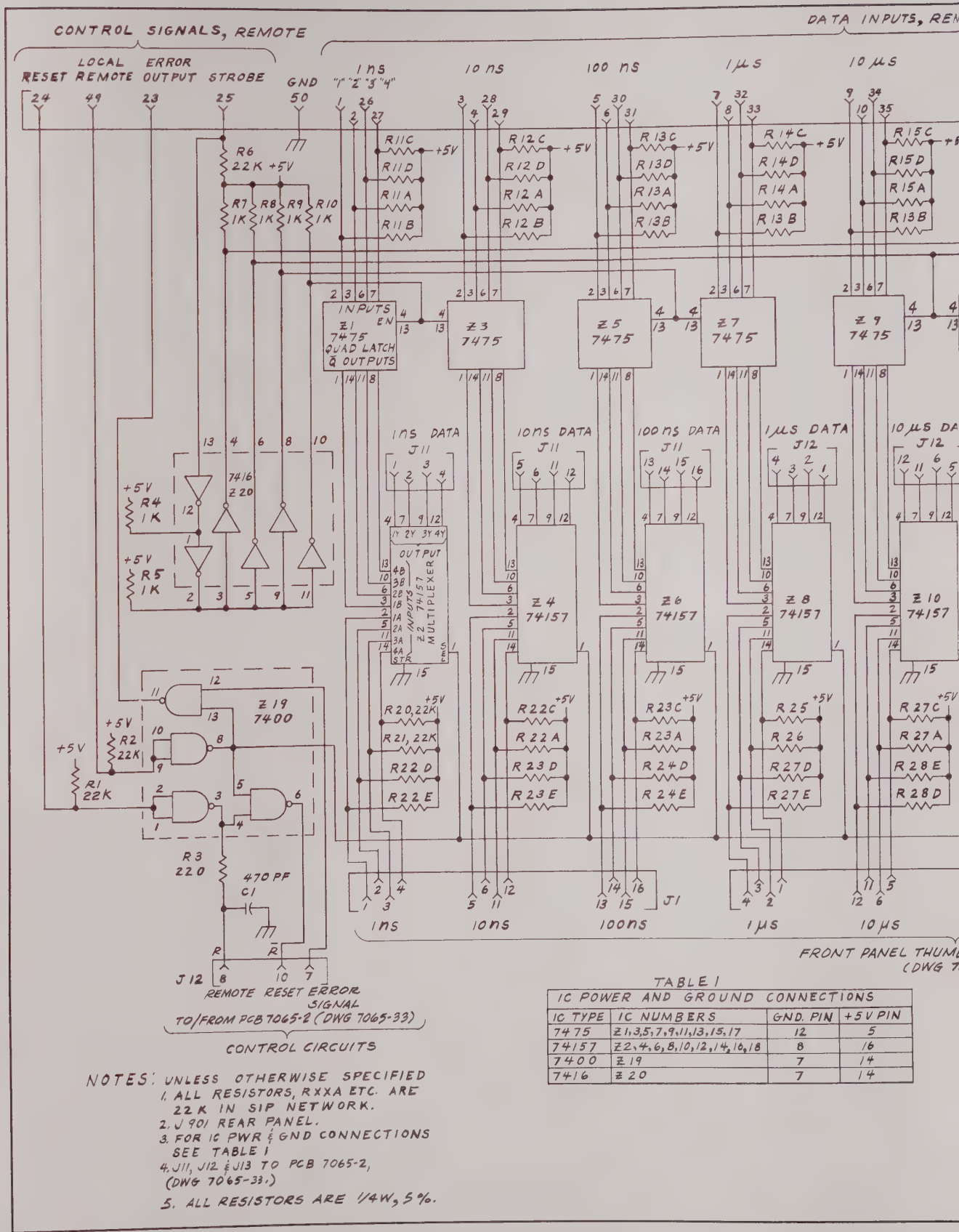
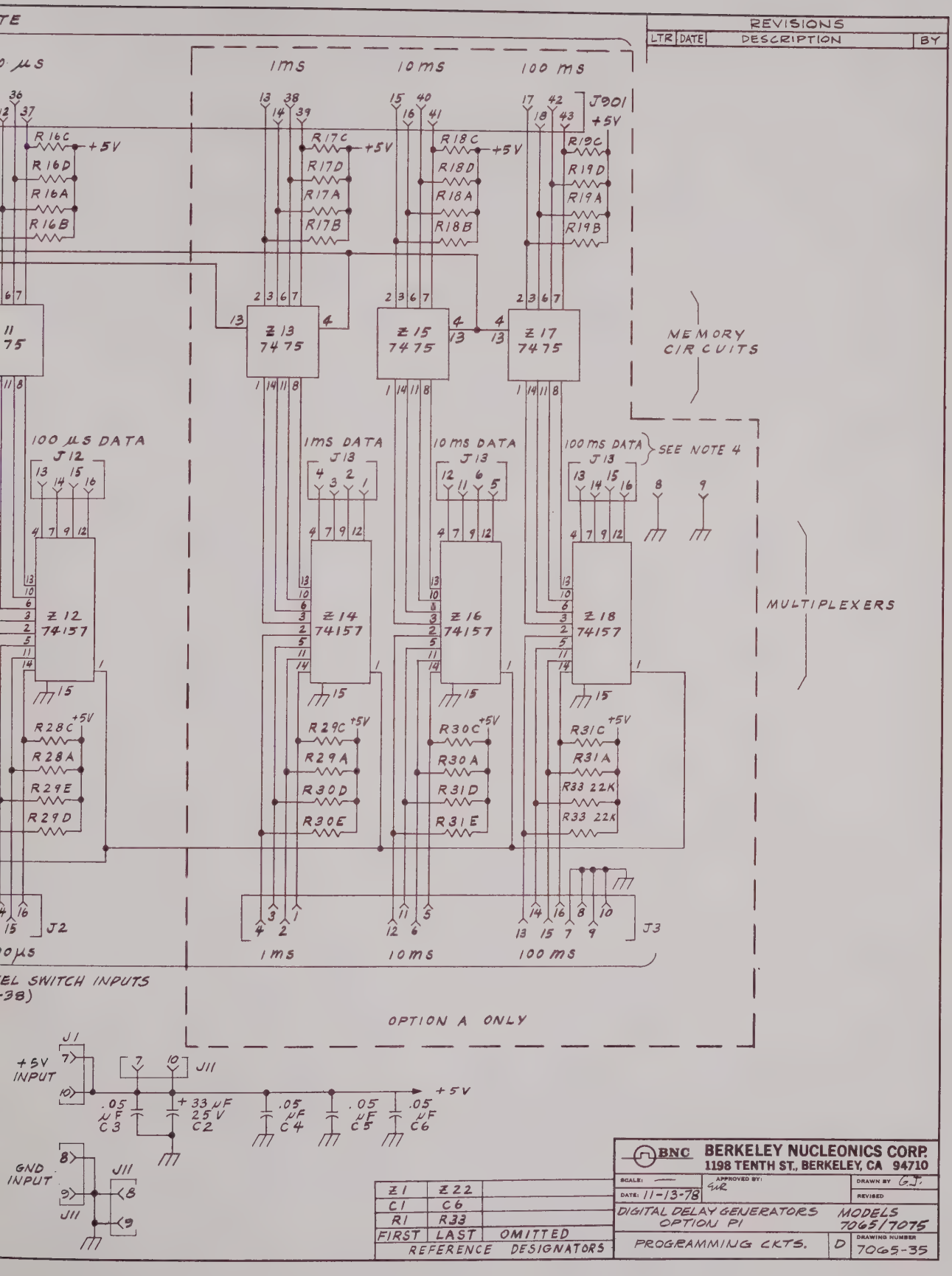


TABLE I

IC POWER AND GROUND CONNECTIONS			
IC TYPE	IC NUMBERS	GND. PIN	+5V PIN
7475	Z1, 3, 5, 7, 9, 11, 13, 15, 17	12	5
74157	Z2, 4, 6, 8, 10, 12, 14, 16, 18	8	16
7400	Z19	7	14
7416	Z20	7	14

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS, RXXA ETC. ARE 22K IN SIP NETWORK.
2. J901 REAR PANEL.
3. FOR IC PWR & GND CONNECTIONS SEE TABLE I
4. J11, J12 & J13 TO PCB 7065-2, (DWG 7065-33.)
5. ALL RESISTORS ARE 1/4W, 5%.



Z1	Z22
C1	C6
R1	R33
FIRST	LAST OMITTED

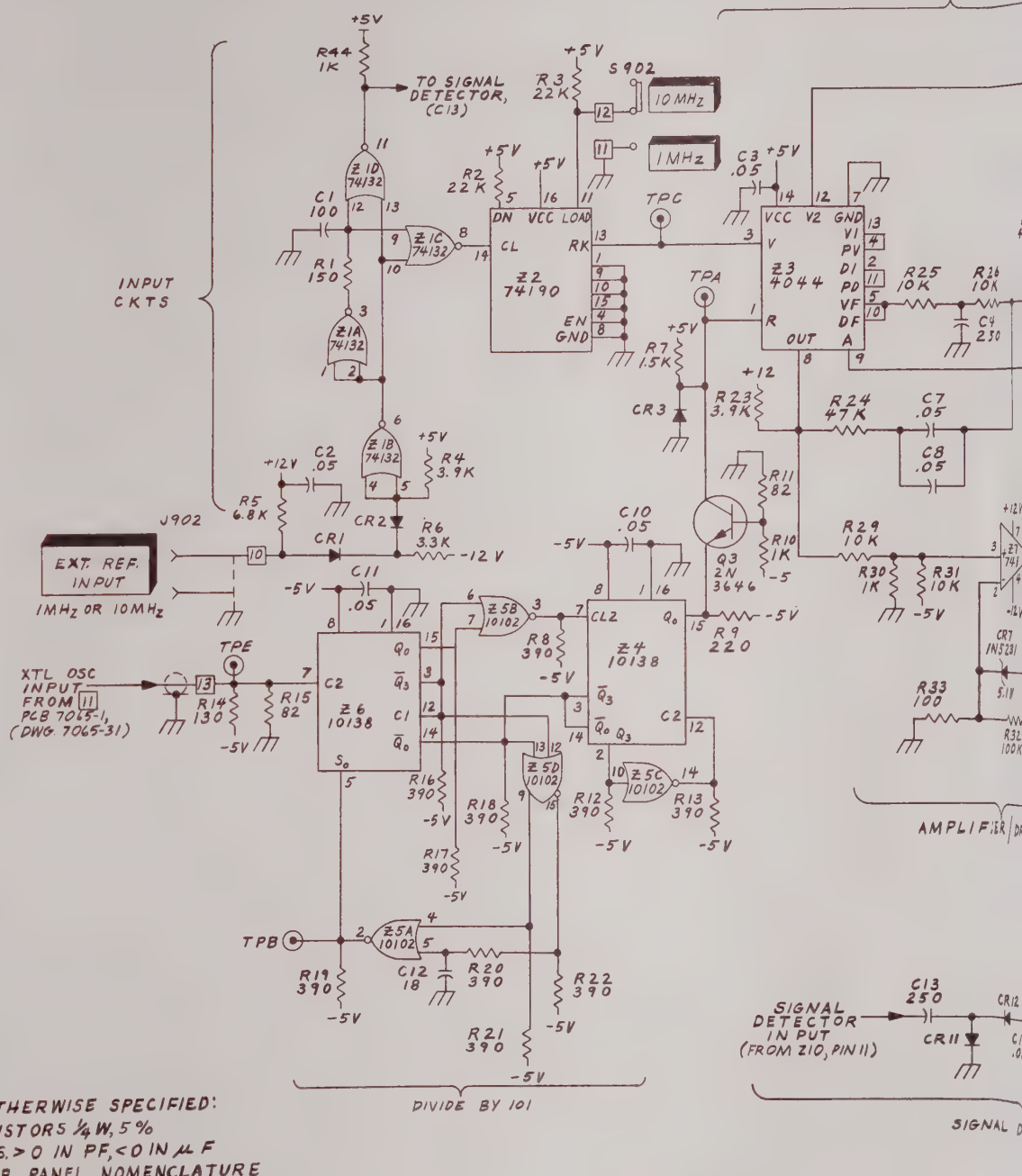
REFERENCE DESIGNATORS

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: — APPROVED BY: GJR DRAWN BY G.J.
DATE: 11-13-78 REVISED

DIGITAL DELAY GENERATORS OPTION P1 MODELS 7065/7075

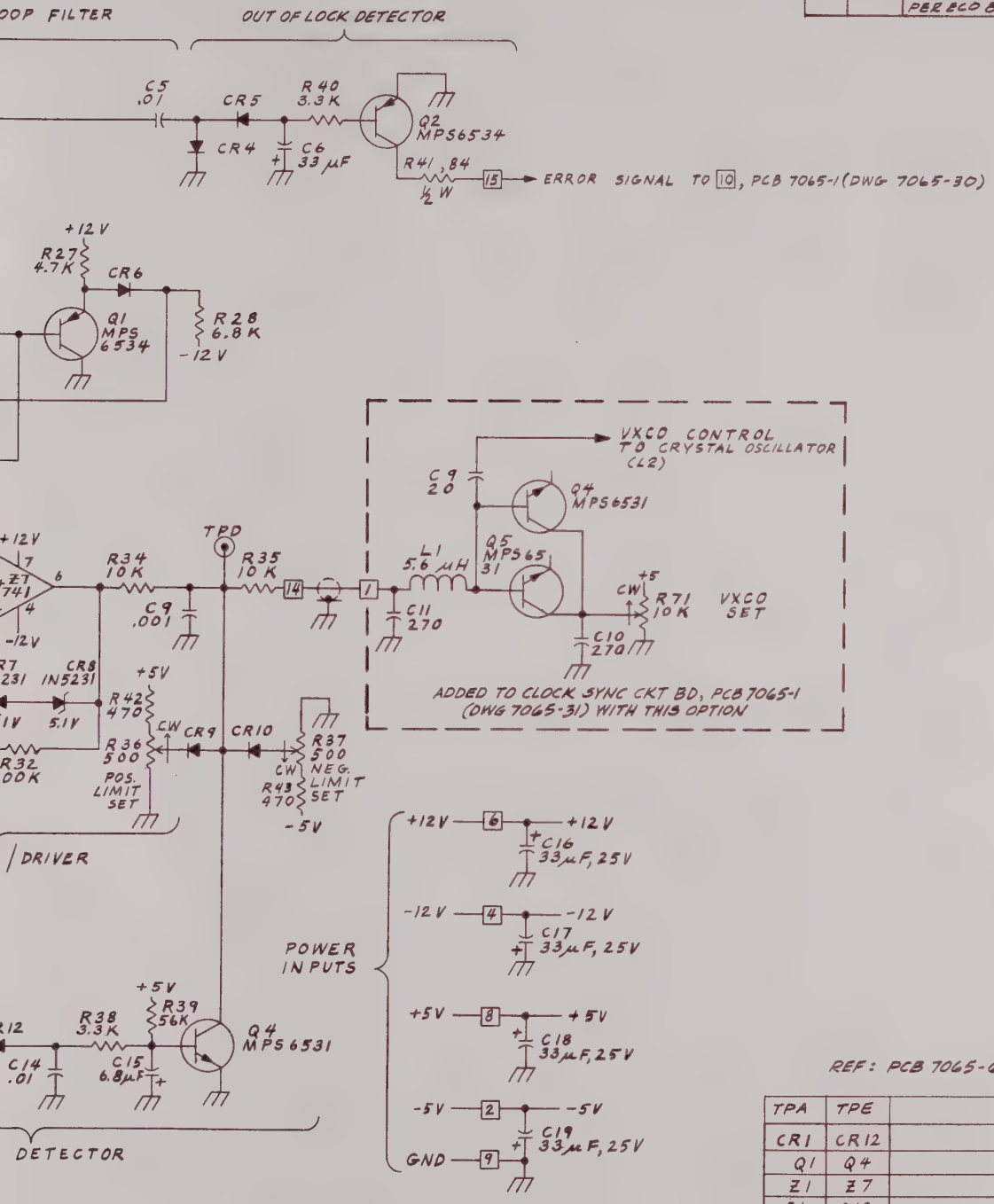
PROGRAMMING CKTS. D DRAWING NUMBER 7065-35



NOTES:
UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ¼W, 5%
2. ALL CAPS. > 0 IN PF, < 0 IN μF
3. ▭ REAR PANEL NOMENCLATURE
4. Z5, 10102 GND = PINS 1, 16; -5V = PIN 8
5. Z1, 74132, GND = PINS 7, +5V = PIN 14
6. ALL DIODES - IN4152
7. □ DENOTES PCB WIRING CONNECTIONS.
8. ⊙ DENOTES TEST POINT

REVISIONS			
LTR.	DATE	DESCRIPTION	BY
A	11-28-78	REDRAWN	G.J.
B	6-18-81	ADD 1K R FRM Z1, PIN 11 TO +5V PER ECO 81-016	



REF: PCB 7065-6

TPA	TPE	
CR1	CR12	
Q1	Q4	
Z1	Z7	
C1	C19	
R1	R44	
FIRST	LAST	OMITTED

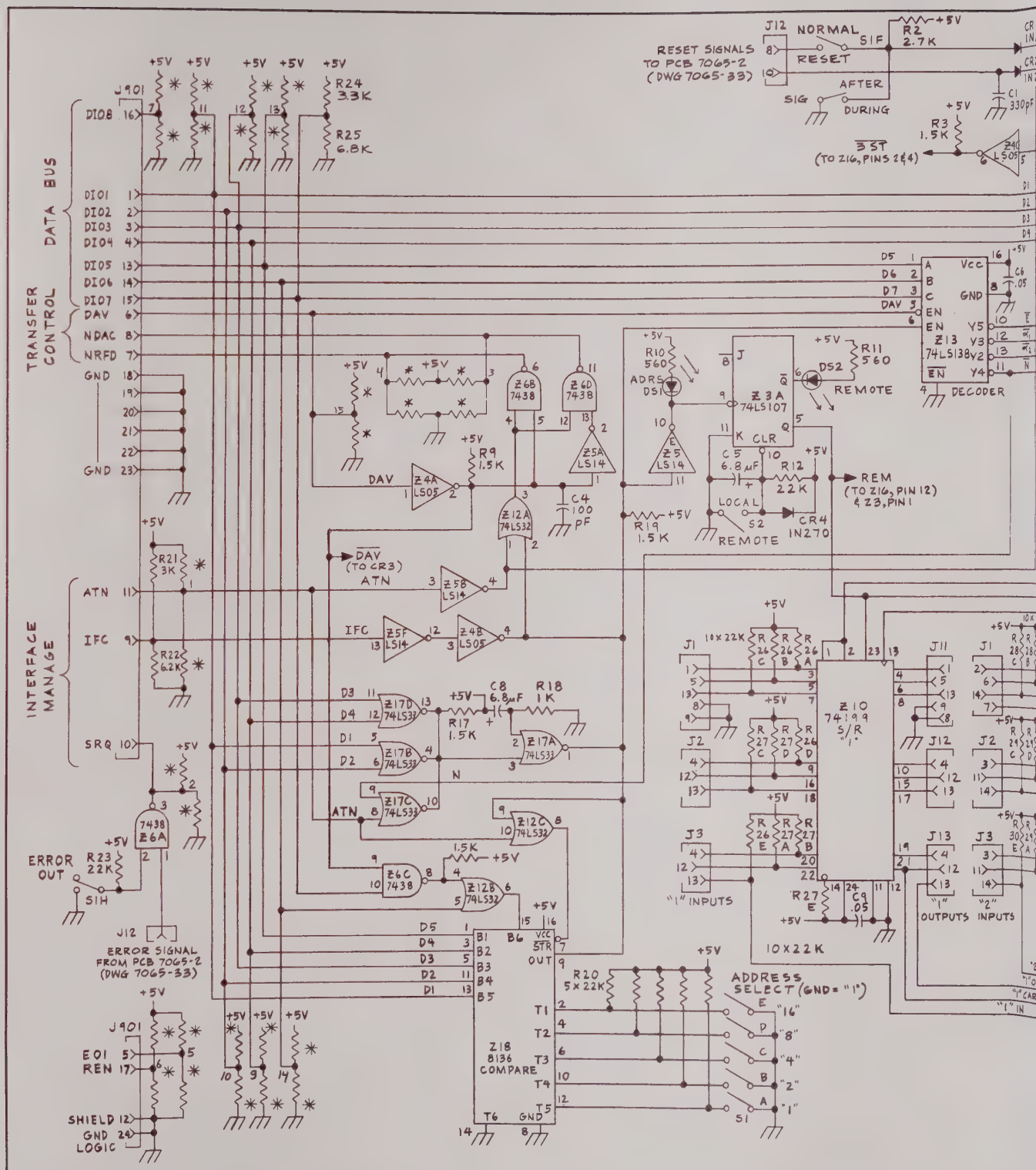
REFERENCE DESIGNATIONS

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE:	APPROVED BY:	DRAWN BY: G.J.
DATE: 11-28-78		REVISED

DIGITAL DELAY GENERATOR
MODEL 7065/7075 OPTION B

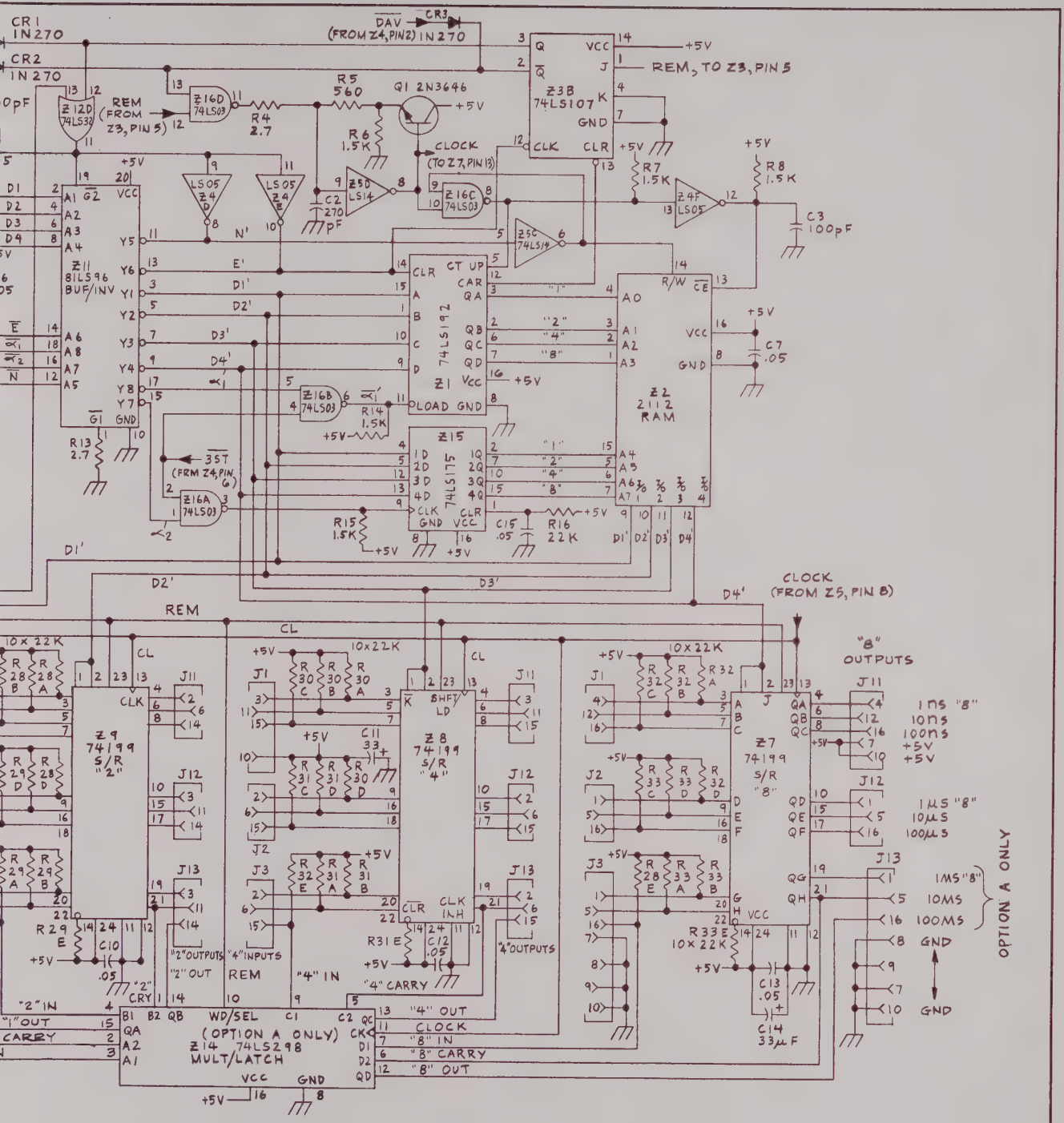
EXTERNAL REFER. CIRCUITS — DRAWING NUMBER 7065-36B



NOTES

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS 1/4 W. 5%.
2. ALL CAP. IN μF.
3. IC'S: PIN 14 IS +5V, PIN 7 IS GND.
4. >— DATA IN/OUT CONNECTORS PINS.
5. * DENOTES R1, 16 PIN DIP NETWORK, PIN 16 (+5V), PIN 8 GND (3.0K TO +5V, 6.2K TO GND AT EACH NODE).
6. J1, J2 & J3 ARE FROM THUMBWHEEL SWITCHES. PCB 7065-B (DWG 7065-38).
7. J11, J12 & J13 ARE DATA OUTPUT TO PCB 7065-2 (DWG 7065-33).



J1, J901	J13, J901	J5 - J10
S1	S2	
Q1	Q1	
DS1	DS2	
Z1	Z18	
CR1	CR4	
C1	C15	
R1	R33	
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

REF: PCB 7065-7

LTR	DATE	DESCRIPTION	BY	CHKD
D	2/10/83	PER ECO 83-006		
C	4/20/82	Z6 & Z16C CHG'D FROM NOR TO NAND GATES PER ECO 80-100		
B	2/17/82	CNG'D R24 FRM 4.7K TO 3.3K, R25 FRM 10K TO 6.8K PER ECO 82-007		
A	8-25-80	PER ECO 80-092		

REVISIONS

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: —
APPROVED BY: Sign 8-27-79
DRAWN BY
DATE: 1-2-79
REVISED

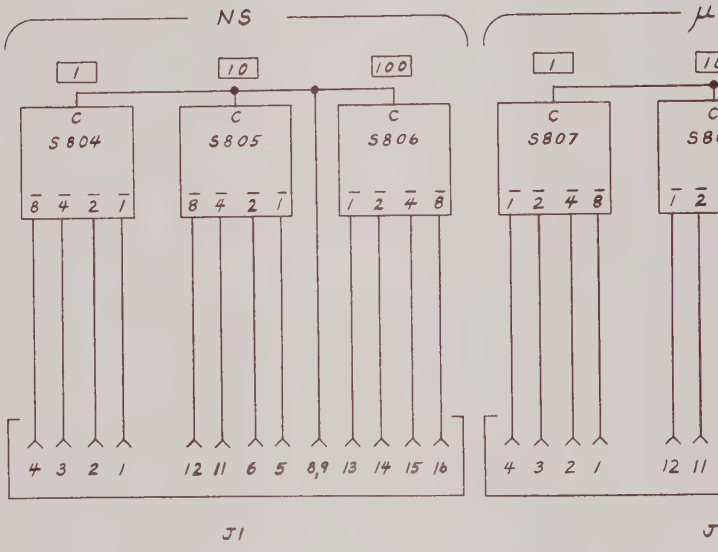
DIGITAL DELAY GENERATORS 7065/7075
OPTION P2

IEEE INTERFACE CIRCUITS

D

DRAWING NUMBER 7065-37D

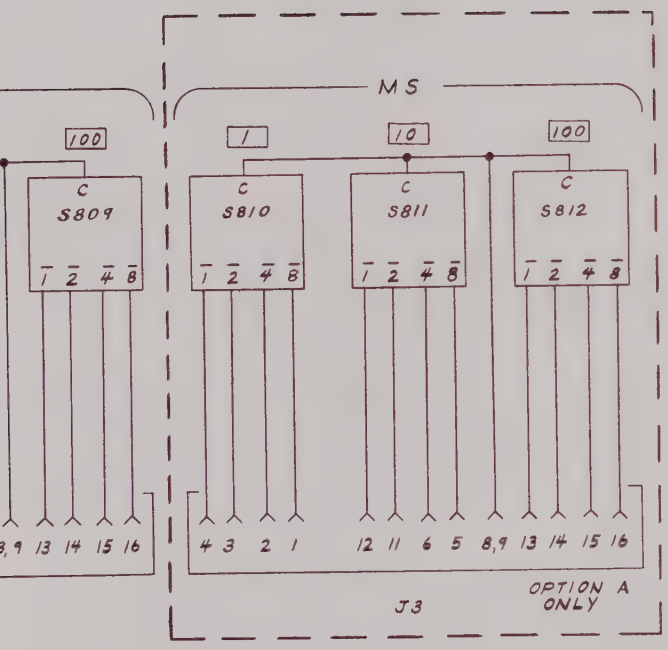
DEL



NOTES

1. ☐ DENOTES FRONT PANEL WORDING

REVISIONS			
DATE	LTR	DESCRIPTION	BY

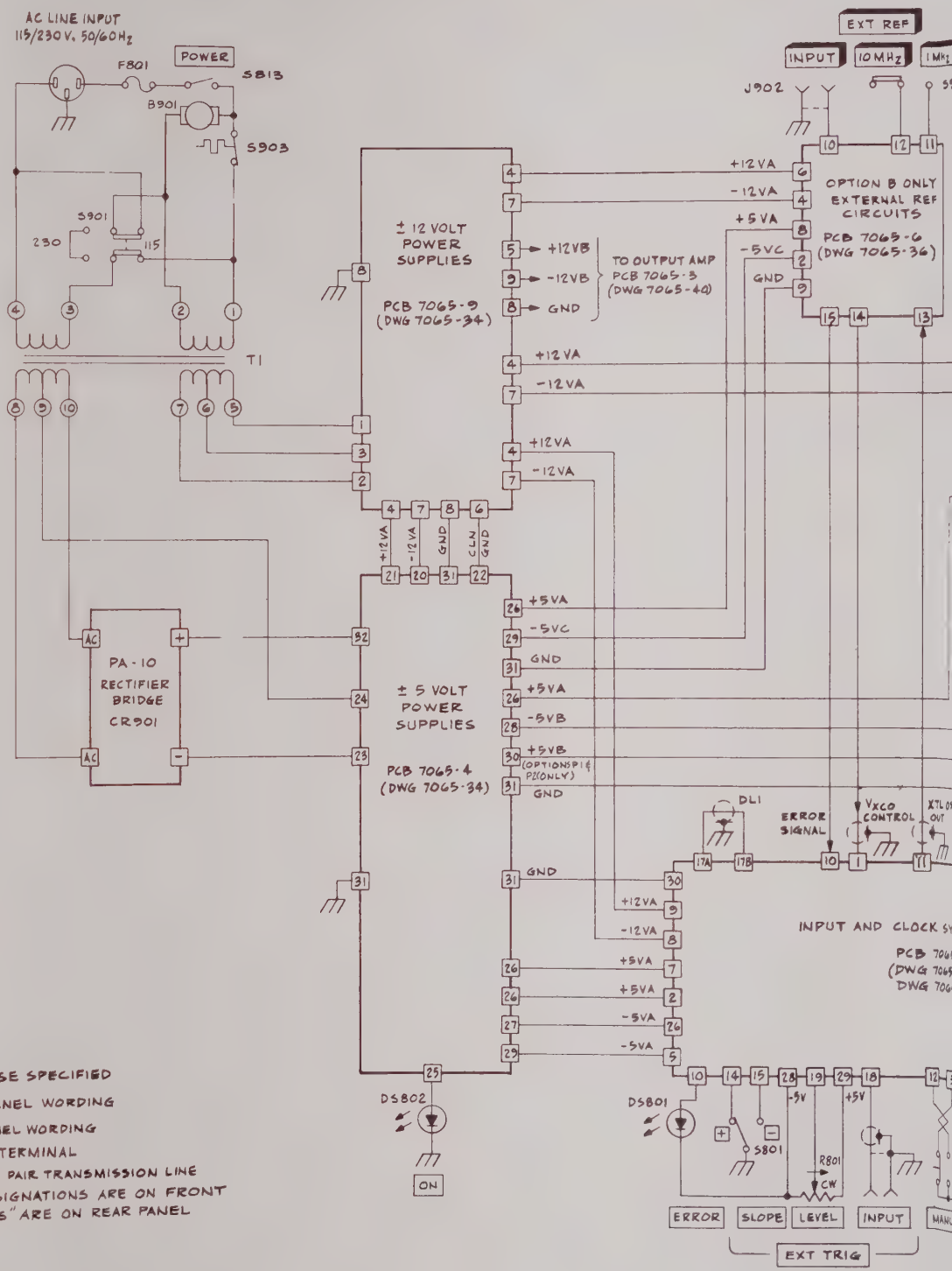


UNTER & INS LINES
G. D-7065-33

RAM BOARD, 7065-5
5 - 35

REF. P.C.BD. - 7065-8

BNC BERKELEY NUCLEONICS CORP. 1198 TENTH ST., BERKELEY, CA 94710		
SCALE: —	APPROVED BY: CWR	DRAWN BY: SG
DATE: 11-1-78		REVISED
DIGITAL DELAY GENERATORS		MODEL 7065/75
THUMBWHEEL SWITCHBD.	D	DRAWING NUMBER 7065-38

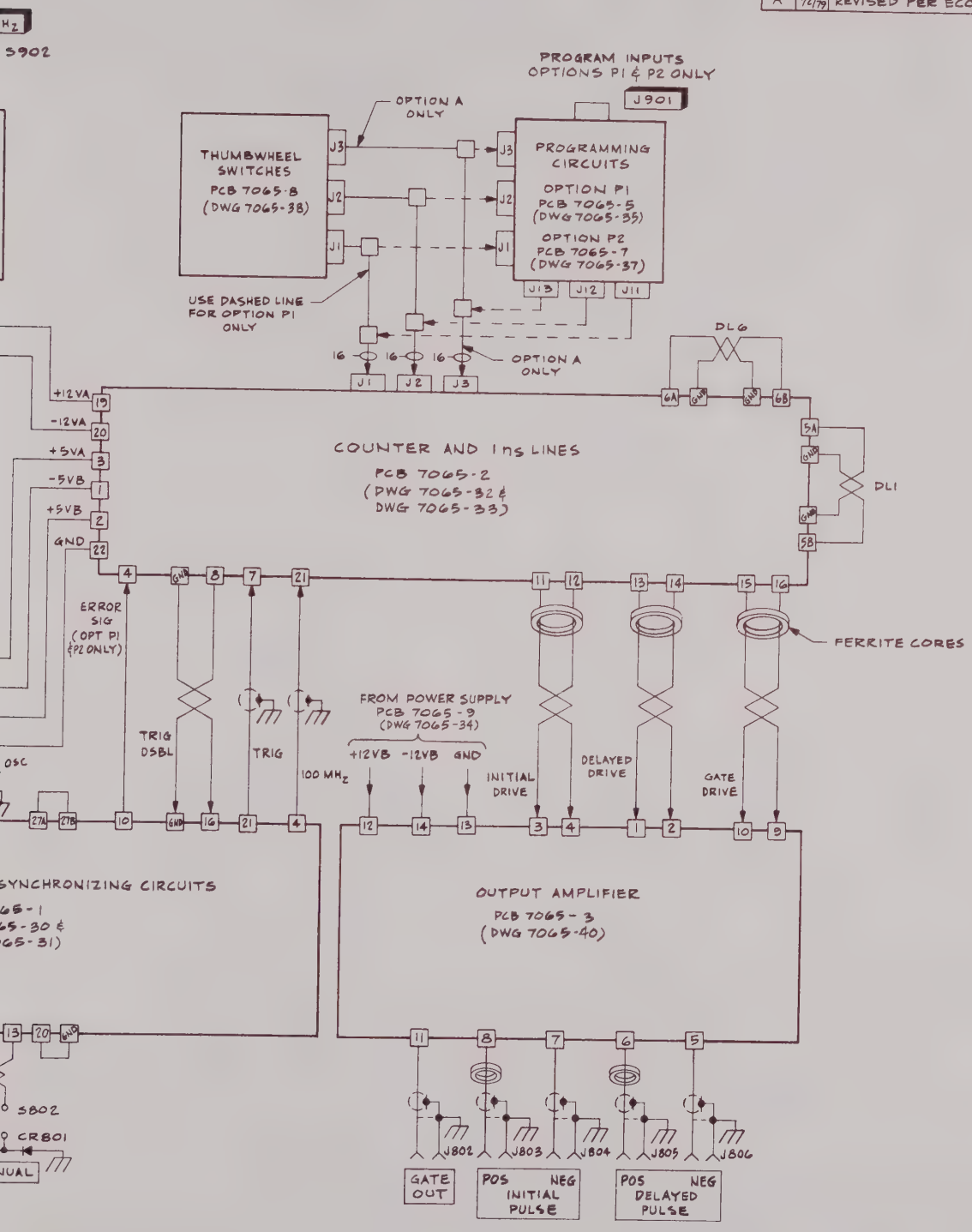


NOTES:

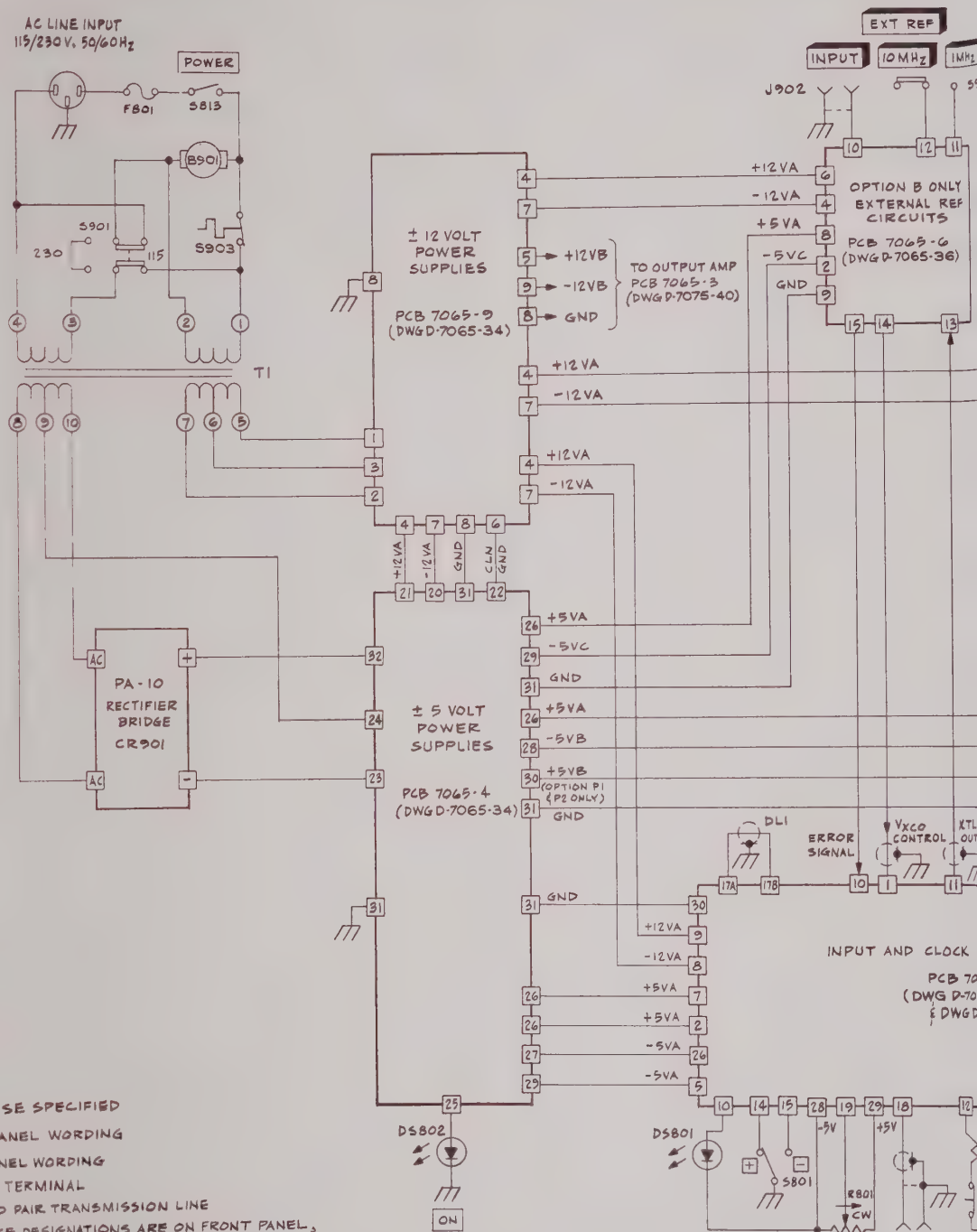
UNLESS OTHERWISE SPECIFIED

1. ▭ FRONT PANEL WORDING
2. ▰ REAR PANEL WORDING
3. □ PC BOARD TERMINAL
4. ⋈ TWISTED PAIR TRANSMISSION LINE
5. "800" REF. DESIGNATIONS ARE ON FRONT PANEL, "900's" ARE ON REAR PANEL

REVISIONS			
LTR	DATE	DESCRIPTION	BY
A	11/2/79	REVISED PER ECO 79-033 & 79-034	LM



BNC BERKELEY NUCLEONICS CORP. 1198 TENTH ST., BERKELEY, CA 94710		
SCALE: NONE	APPROVED BY: CMK	DRAWN BY: LM
DATE: 6/20/78		REVISED
DIGITAL DELAY GENERATOR MODEL 7065		
INTERCONNECTION DIAGRAM	D	DRAWING NUMBER 7065-39A

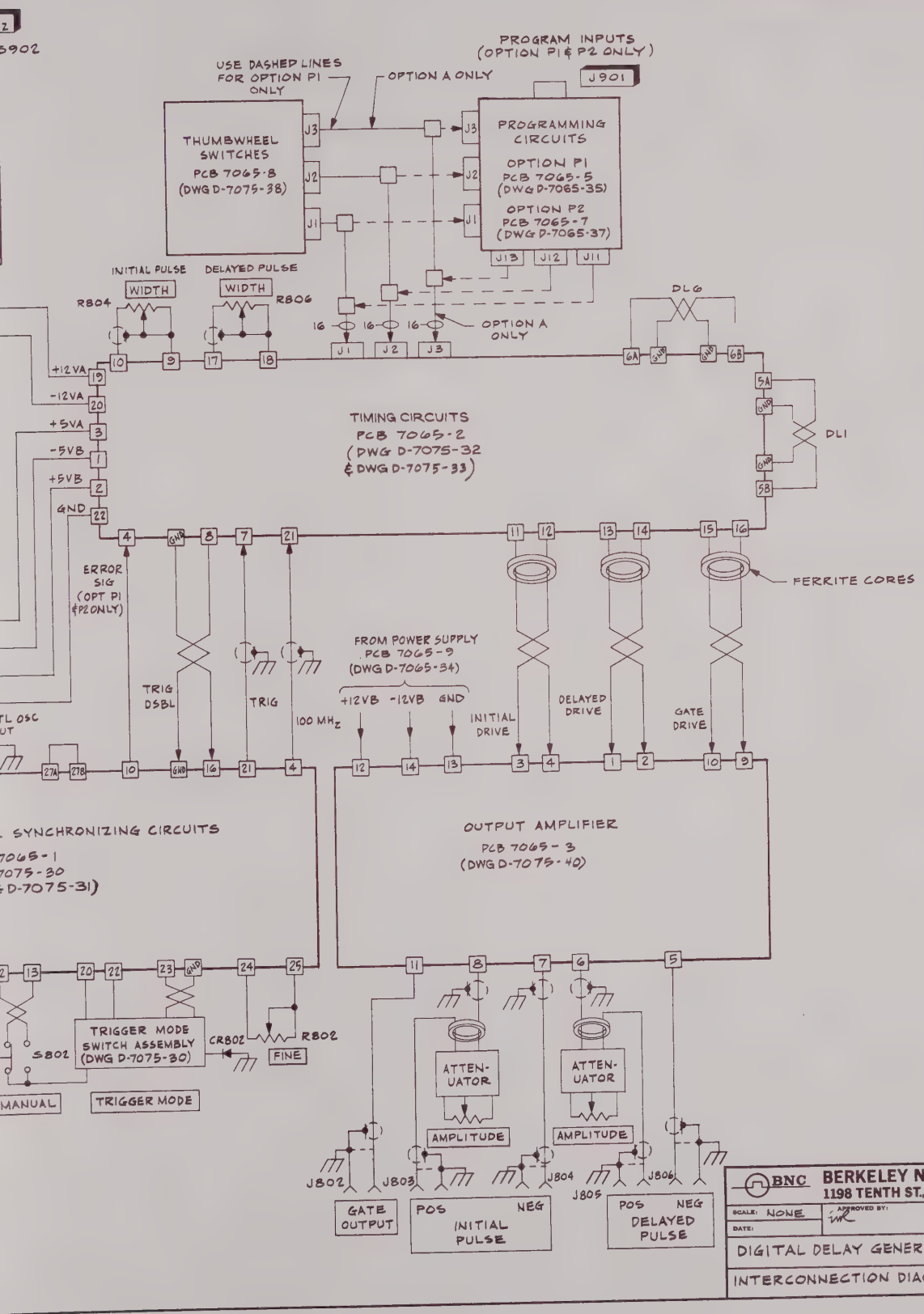


NOTES:

UNLESS OTHERWISE SPECIFIED

1. ▭ FRONT PANEL WORDING
2. ▰ REAR PANEL WORDING
3. □ PC BOARD TERMINAL
4. ⋈ TWISTED PAIR TRANSMISSION LINE
5. "800" REFERENCE DESIGNATIONS ARE ON FRONT PANEL, "900" REFERENCE DESIGNATIONS ARE ON REAR PANEL.

REVISIONS				
LTR	DATE	DESCRIPTION	BY	CHKD
A	6-17-80	PER ECO 79-034	RLP	
B	7-8-80	PER ECO'S 80-078 & 80-081	RLP	

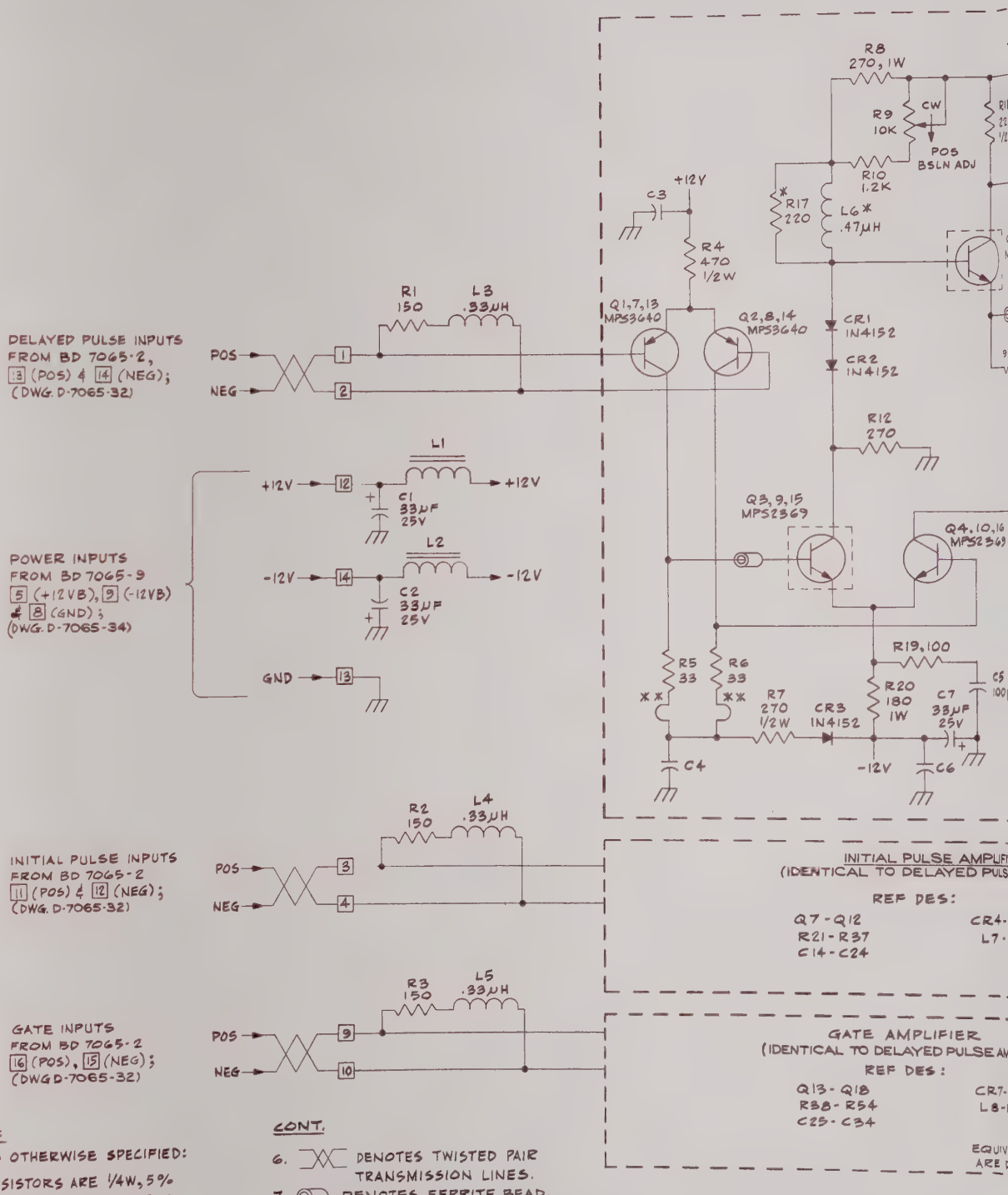


BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE: NONE	APPROVED BY:	DRAWN BY
DATE:		REVISED

DIGITAL DELAY GENERATOR MODEL 7075

INTERCONNECTION DIAGRAM D DRAWING NUMBER 7075-39B



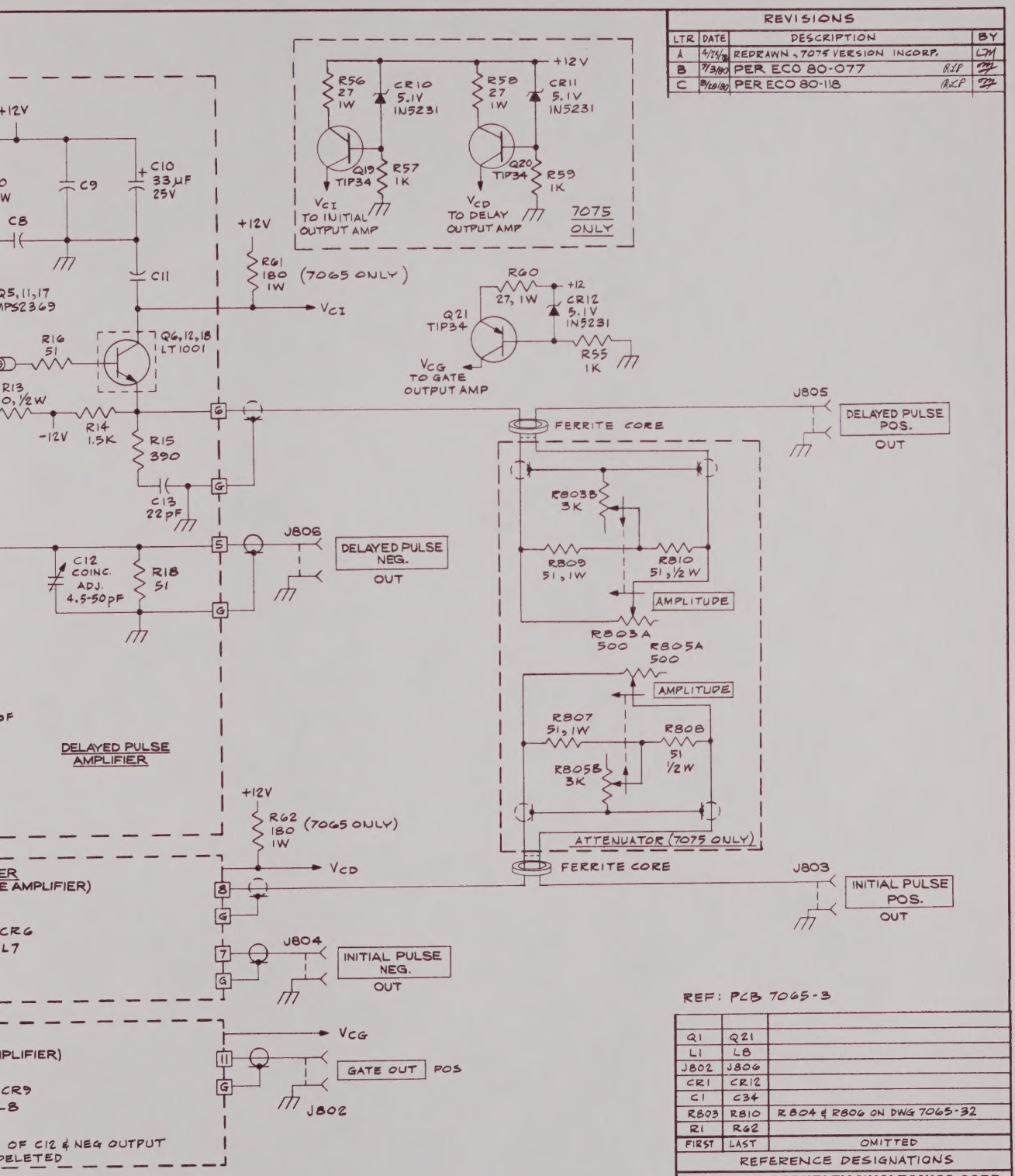
NOTES:

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 1/4W, 5%
   ALL CAPACITORS ARE .05µF
2. * FACTORY SELECTED PART-NOMINAL VALUE SHOWN.
3. ** INDUCTOR FORMED BY RESISTOR LEADS.
4. --- INDICATES TRANSISTOR HAS HEAT SINK.
5. L1 & L2: 10 TURNS ON FERRITE CORE
   BNC PART NO. 318-004.

CONT.

6. DENOTES TWISTED PAIR TRANSMISSION LINES.
7. DENOTES FERRITE BEAD.
8. DENOTES PCB WIRING CONNECTION.
9. DENOTES FRONT PANEL WORDING.


REVISIONS
LTR DATE DESCRIPTION BY
A 4/24/78 REDRAWN, 7075 VERSION INCORP. LTM
B 7/3/80 PER ECO 80-077 RSP
C 9/26/80 PER ECO 80-118 RSP
+12V
R56 27 1W
CR10 5.1V IN5231
R58 27 1W
CR11 5.1V IN5231
Q19 TIP34
R57 1K
Q20 TIP34
R59 1K
VCI TO INITIAL OUTPUT AMP
VCD TO DELAY OUTPUT AMP
7075 ONLY
C9
C10 33µF 25V
C8
C11
R61 180 1W (7065 ONLY)
VCI
R60 27, 1W
+12
CR12 5.1V IN5231
Q21 TIP34
R55 1K
VCG TO GATE OUTPUT AMP
Q6,12,18 LT1001
R16 51
R13 0, ½W
-12V
R14 1.5K
R15 390
C13 22pF
J805
DELAYED PULSE POS. OUT
FERRITE CORE
R803B 3K
R809 51, 1W
R810 51, ½W
AMPLITUDE
R803A 500
R805A 500
AMPLITUDE
R807 51, 1W
R808 51 ½W
R805B 3K
ATTENUATOR (7075 ONLY)
FERRITE CORE
J806
DELAYED PULSE NEG. OUT
C12 COINC. ADJ. 4.5-50pF
R18 51
DELAYED PULSE AMPLIFIER
+12V
R62 180 1W (7065 ONLY)
VCD
J803
INITIAL PULSE POS. OUT
J804
INITIAL PULSE NEG. OUT
VCG
GATE OUT POS
J802
REF: PCB 7065-3
Q1 Q21
L1 L8
J802 J806
CR1 CR12
C1 C34
R803 R810 R804 & R806 ON DWG 7065-32
R1 R62
FIRST LAST OMITTED
REFERENCE DESIGNATIONS
BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710
SCALE: NONE
APPROVED BY: Gwr 3-25-79
DRAWN BY LTM
DATE: 4-25-78
REVISED
DIGITAL DELAY GENERATOR MODEL 7065/7075
OUTPUT AMPLIFIER CKTS
D
DRAWING NUMBER 7065-40C